

Compal confidential

Thin & Light

NDU01/NDU11 LA-6032P REV 1.0 Schematics Document

Mobile AMD ASB2/RS880M/SB820M

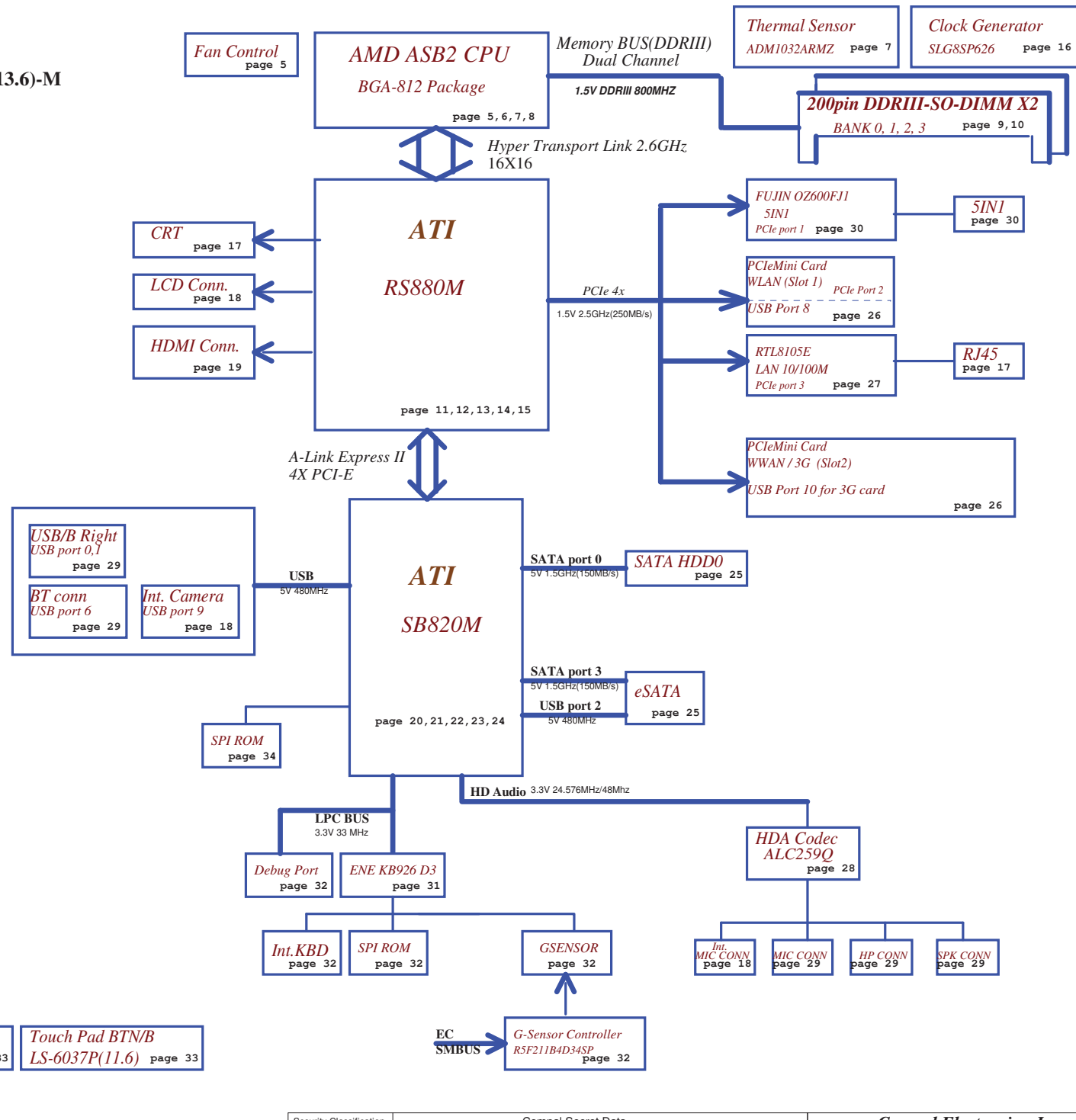
2010-03-22 Rev. 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	Cover Sheet	
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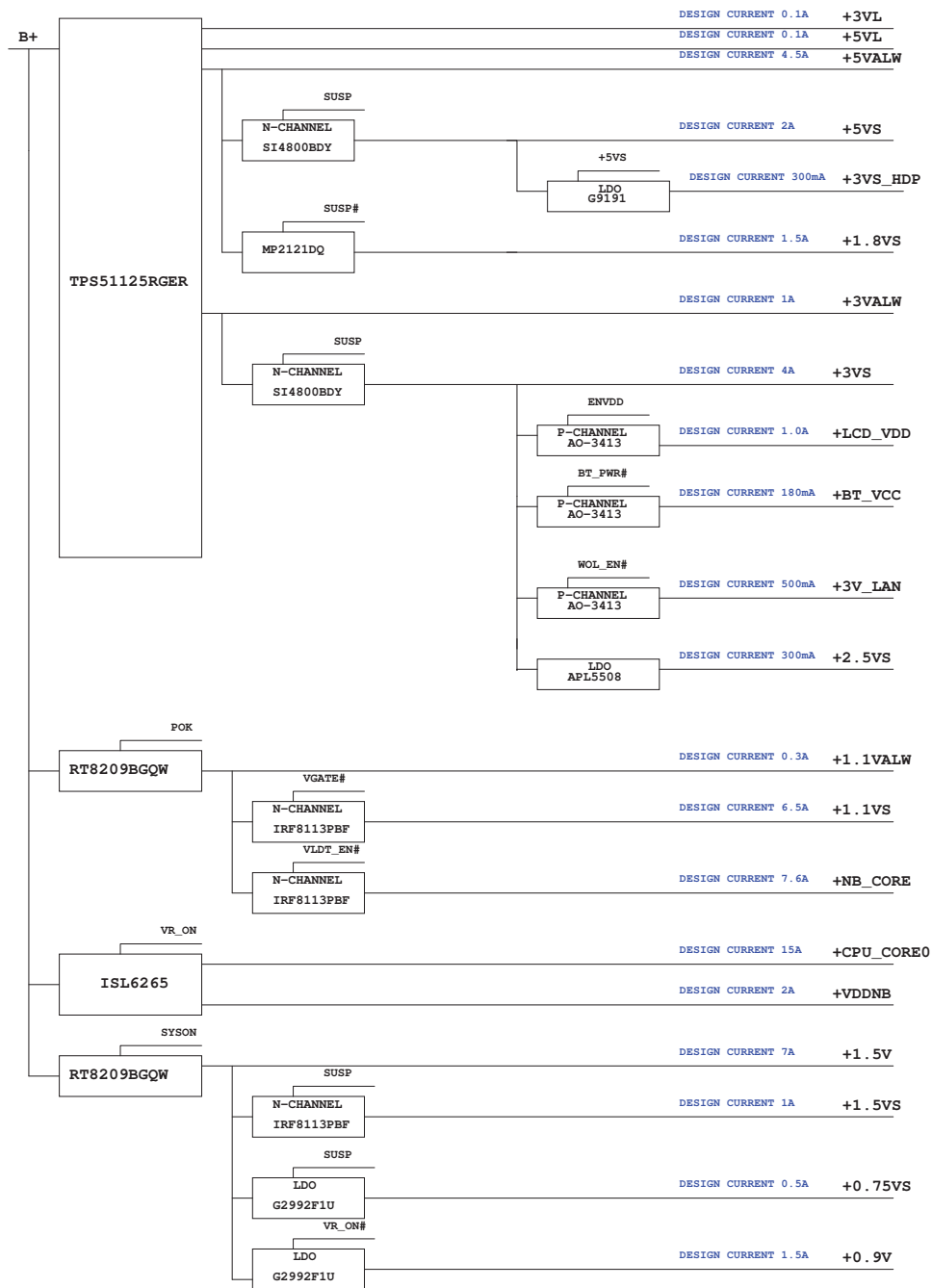
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Model Name : NDU01(11.3)-S/NDU11(13.6)-M

File Name : LA-6032P



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	Title	Block Diagram
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Issued Date	2008/04/14	Deciphered Date	2009/04/14	Title	Power Map
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Voltage Rails

○ MEANS ON X MEANS OFF

power plane State	B+ +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +0.9VS +0.75VS +NB_CORE +VDDNB +CPU_CORE_0
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	X
S5 S4/AC	○	○	X	X
S5 S4/ Battery only	○	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build
 K625R3@ : means just for 1.5G CPU
 K125R3@ : means just for 1.7G CPU
 K325R3@ : means just for 1.3G CPU
 K625R1@ : means just for 1.5G CPU
 K125R1@ : means just for 1.7G CPU
 K325R1@ : means just for 1.3G CPU
 M@ : means just reserve for 13.3 control
 S@ : means just reserve for 11.6 control
 GSENSOR@ : means just reserve for G sensor part
 1ST@ : means just reserve 1st G sensor IC
 1STGSENSOR@ : means just reserve 1st G sensor IC
 2ND@ : means just reserve 2nd G sensor IC
~~2NDGSENSOR@ : means just reserve 2nd G sensor IC~~
 NOSIDE@ : means just reserve NOSIDE
 SIDE@ : means just reserve SIDE port
 RS880MR1@ : means just for RS880MR1
 RS880MR3@ : means just for RS880MR3
 SB820MR1@ : means just for SB820MR1
 SB820MR3@ : means just for SB820MR3

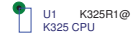
For 11.6 and 13.3 DAZ



K125 mean 1.7G CPU



K325 mean 1.3G CPU



K625 mean 1.7G CPU



K125 mean 1.7G CPU



K325 mean 1.3G CPU



RS880M



SB820M



SB SM Bus1 Address

SB SM Bus2 Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b

Power	Device	HEX	Address
+3VALW	WLAN/WIMAX		

EC SM Bus1 Address

EC SM Bus2 Address

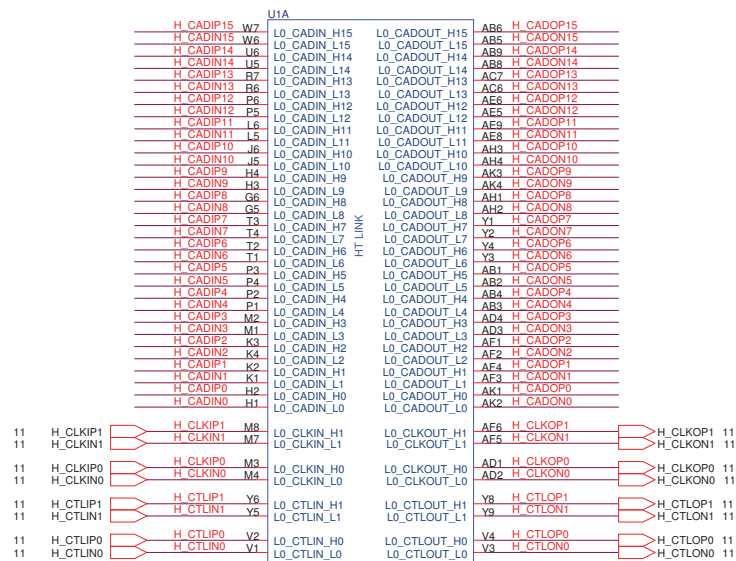
Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 011X b

Power	Device	HEX	Address
+3VS	CPU_ADM1032-1	98 H	1001 100X b
+3VS	G-Sensor		

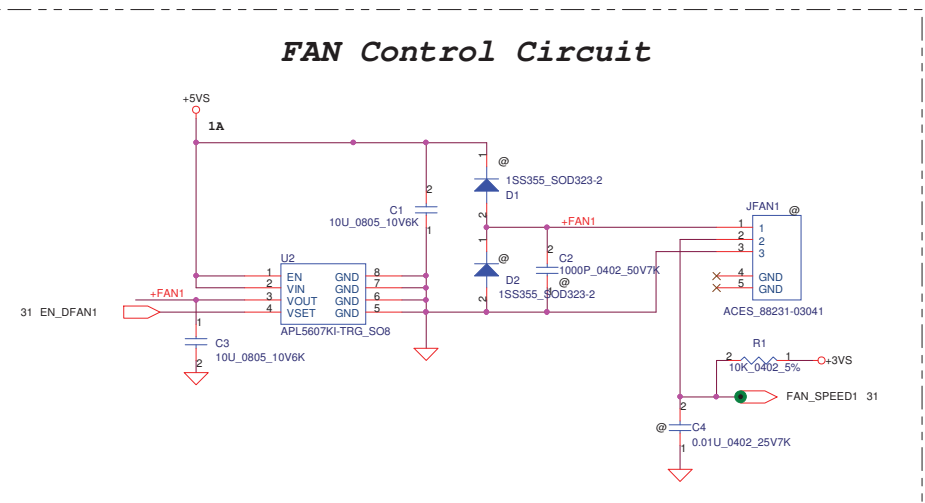
SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM	G-sensor
EC_SMB_CK1	KB926	V							
EC_SMB_DA1									
EC_SMB_CK2	KB926		V						V
EC_SMB_DA2									
I2C_CLK	RS880M						V		
I2C_DATA									
DDC_CLK0	RS880M							V	
DDC_DATA0									
SCL0	SB820			V	V				
SDA0									
SCL1	SB820								
SDA1						V			

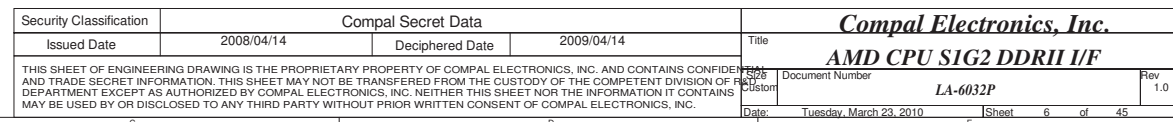
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2008/04/14	Deciphered Date	2009/04/14	Title	Notes List	
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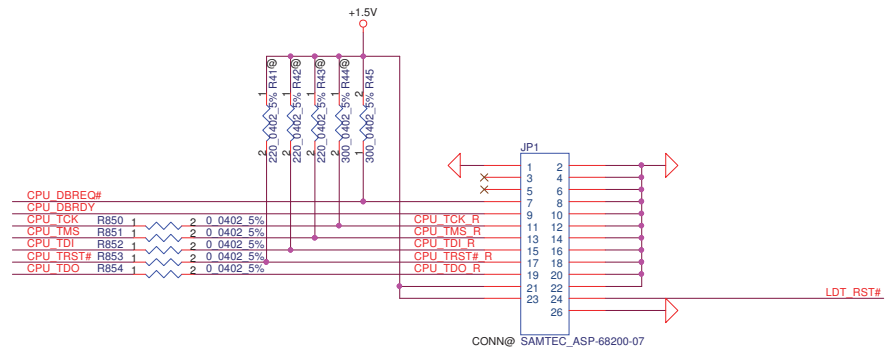
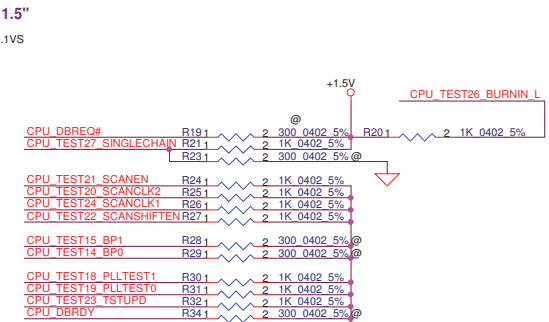
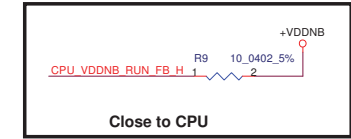
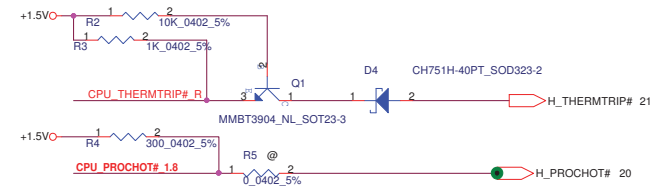
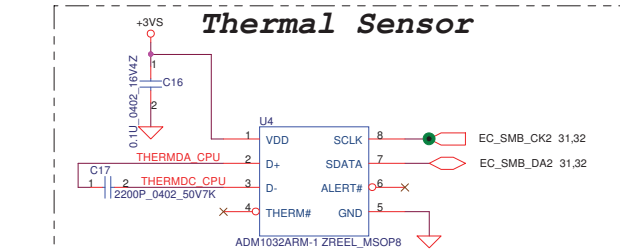
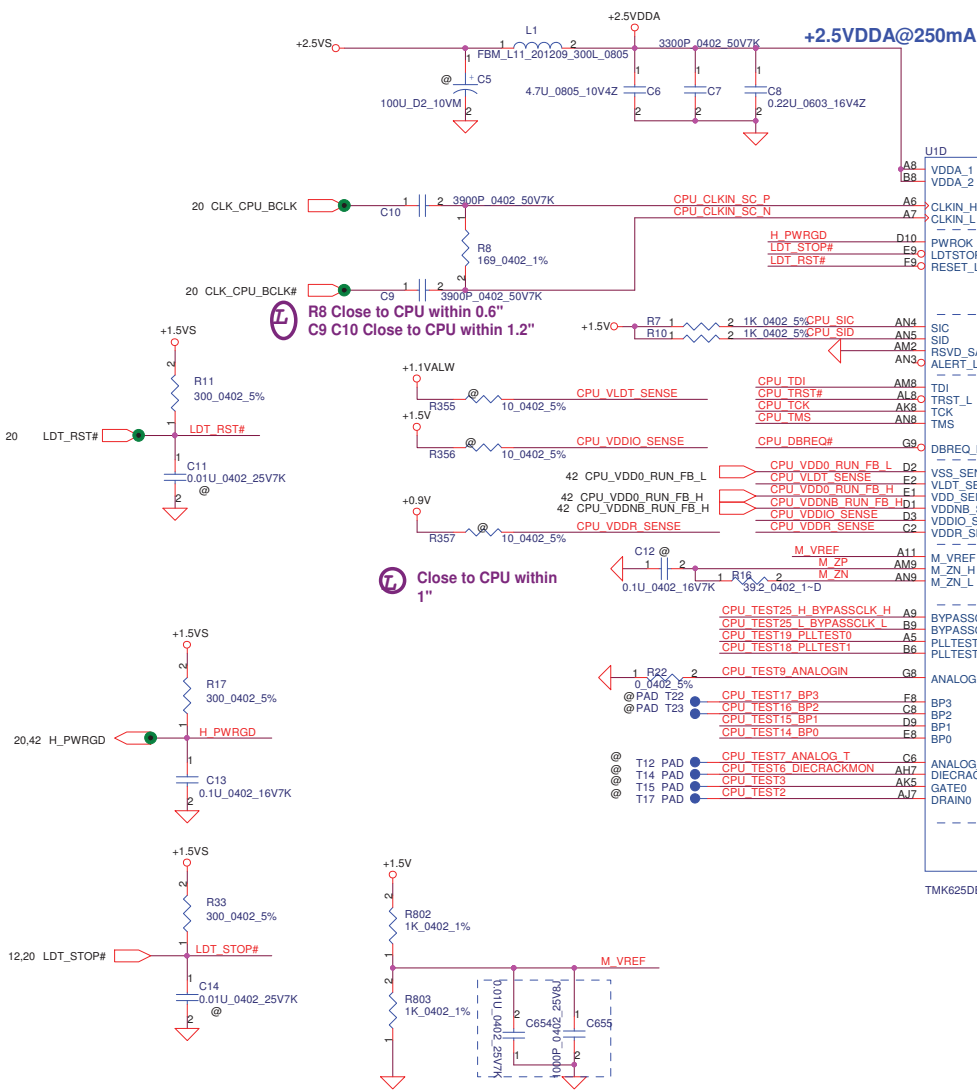


TMK625DBV23GM_FCBGA812
K625@



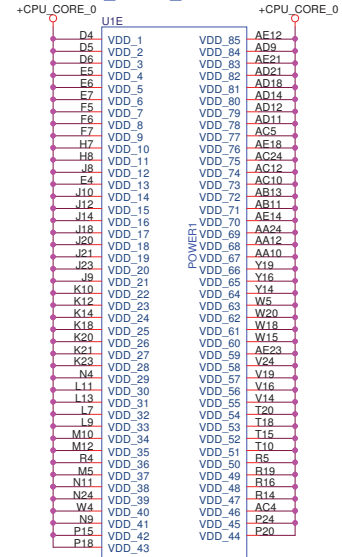
Security Classification		Compal Secret Data		Compal Electronics, Inc. AMD CPU SIG2 HT I/F	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	Title	
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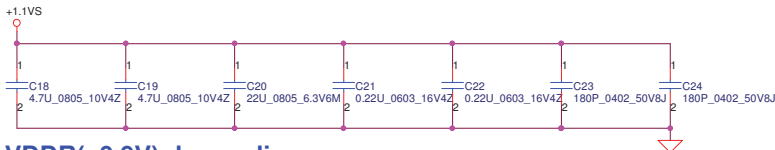
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	Title	AMD CPU SIG2 CTRL
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+CPU_CORE_0@1500mA

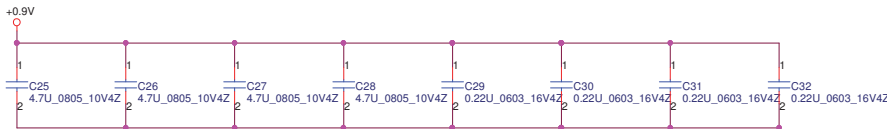


3000mA

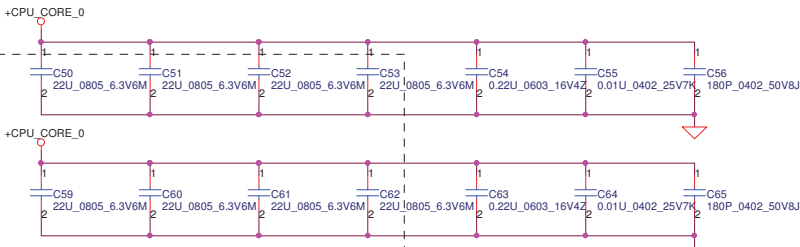
VLDT_A&VLDT_B(+1.1VS) decoupling.



VDDR(+0.9V) decoupling.



VDD(+CPU_CORE_0) decoupling.



CPU BOT site

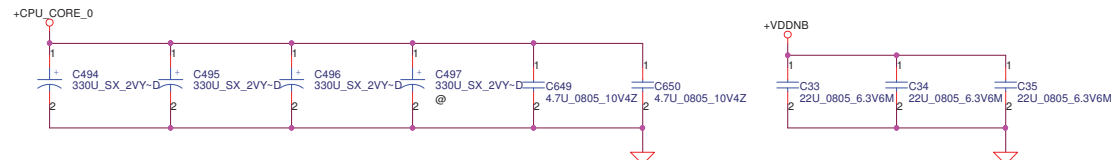
<http://hobi-elektronik.net>

+1.1VS@1500mA

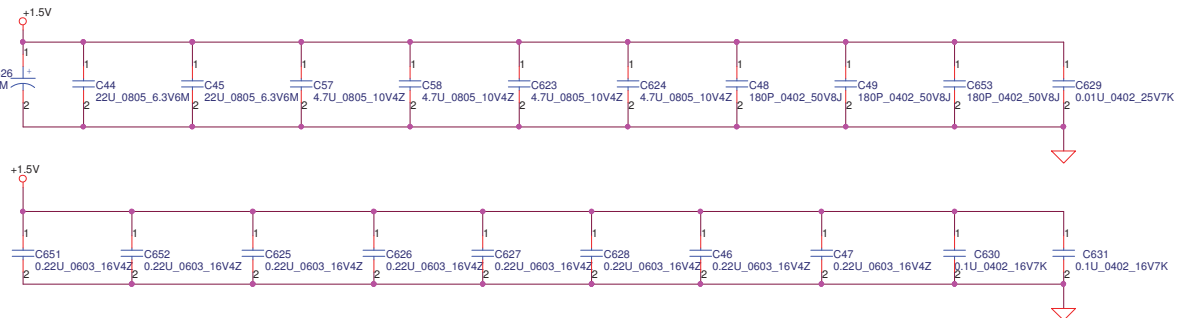
+0.9V@1250mA

+VDDNB@2000mA

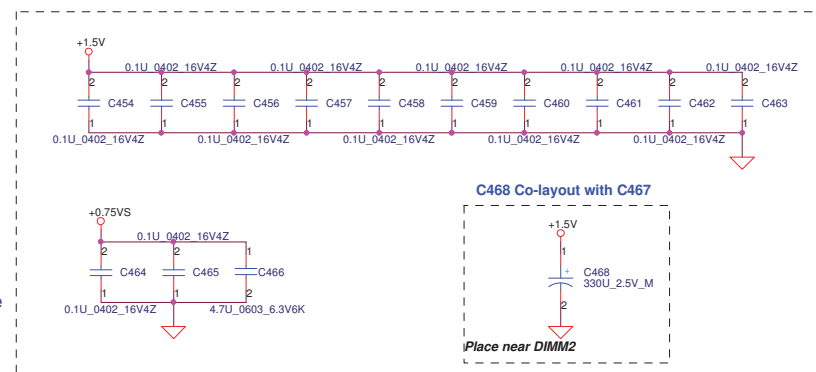
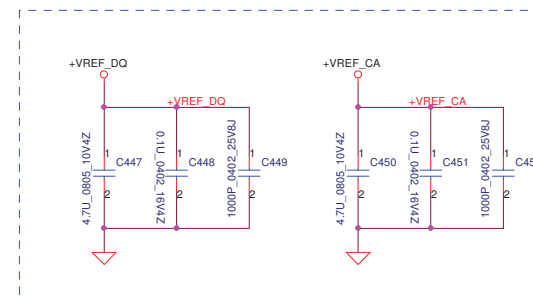
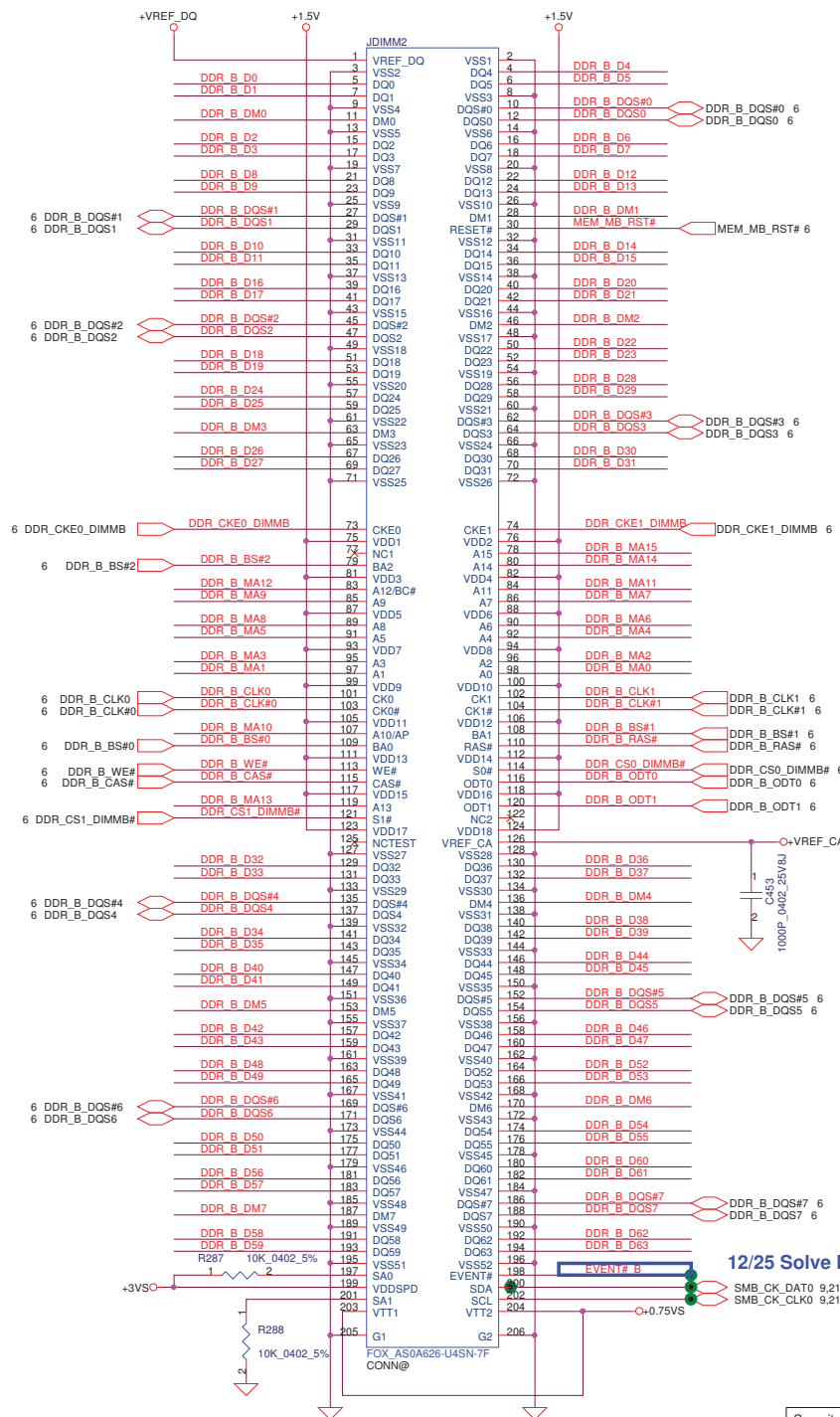
VDD(+CPU_CORE_0) decoupling.



VDDIO(+1.5V) decoupling.



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DIMM_B STD H:4mm
<Address: 01>

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< To Card crader >
< To WLAN >
< To LAN >

< From SB820 : x4 PCIE A-link >

H_CADIP0[0..15] 5
H_CADIN0[0..15] 5

< From S1G4 CPU : x16 HT >

Place within 1" layout 1:2

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

RS880M_FCBGA528

PART 1 OF 6

HYPER TRANSPORT CPU I/F

RS880M_FCBGA528

RS880MR1@

AC1-
AC2-
AC3-
AC4-
AC5-
AC6-
AC7-
AC8-
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AC98-
AC99-
AC100-

R51 within U5 1"
R54 within U5 1"

< To S1G4 CPU : x16 HT >

Place within 1" layout 1:2

HDMI

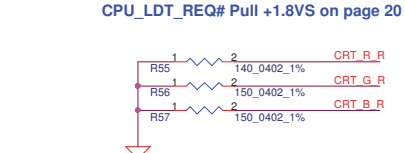
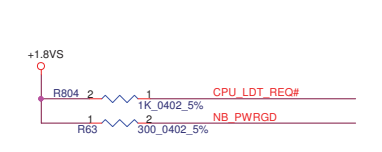
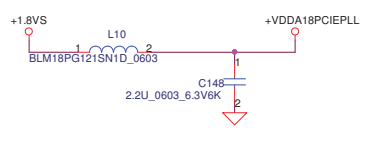
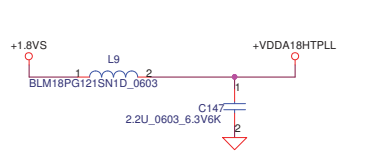
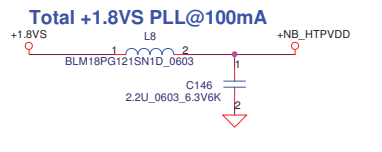
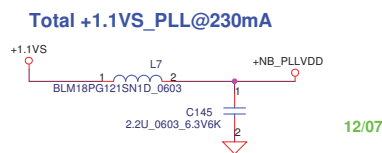
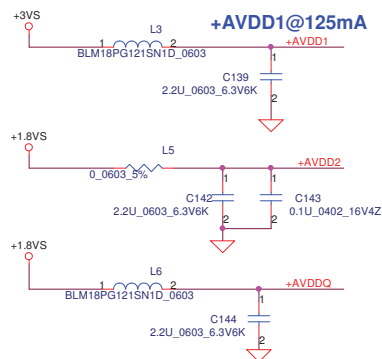
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< To LAN >
< To WWAN >

< To SB820 : x4 PCIE A-link >

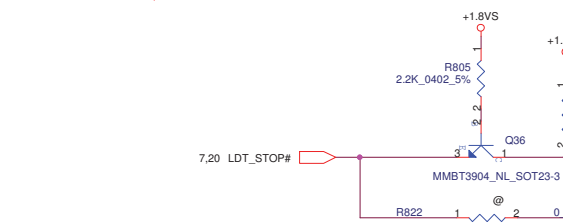
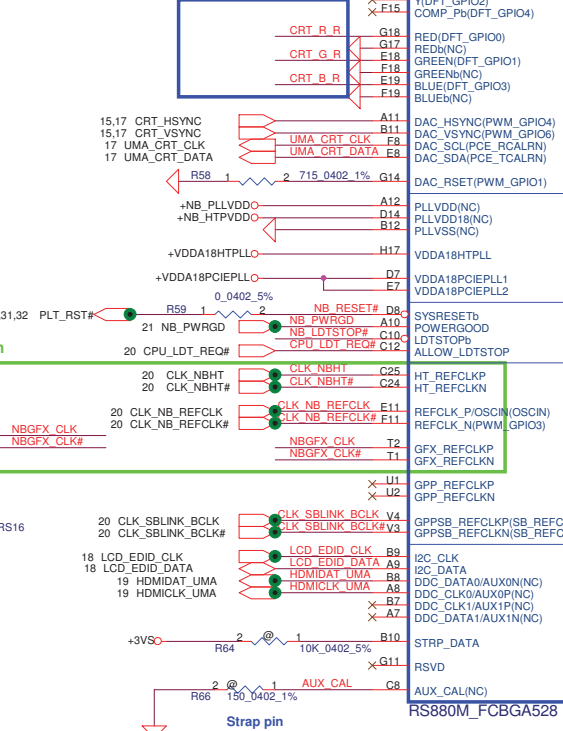
< TX Impedance Calibration. Connect to GND >
< RX Impedance Calibration. Connect to VDDPCIE >

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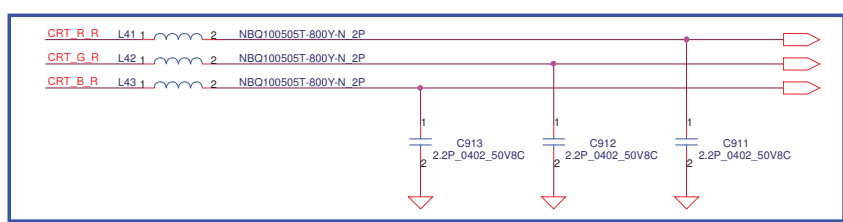
Title		Compal Electronics, Inc.	
RS880M HT/PCIE		Rev 1.0	
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2/2 Fine tune pin define

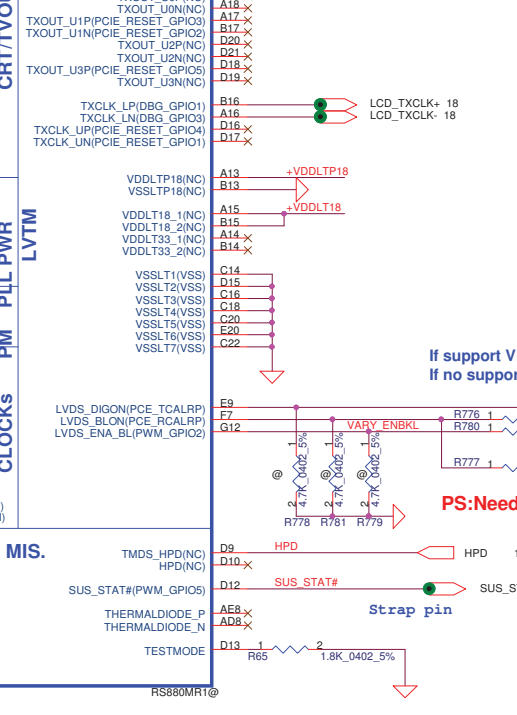


Contact with NB signal



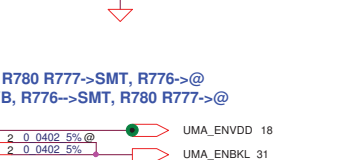
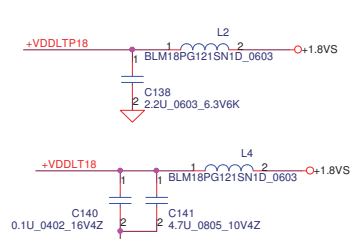
2/2 Add L41 L42 L43 C911 C912 C913 for EMI request

2/2 Fine tune pin define



Contact to CRT conn signal

+VDDLTP18@220mA



If support VB, R780 R777-->SMT, R776-->@
If no support VB, R776-->SMT, R780 R777-->@

PS:Need to fine tune R783 and R784 on Page17

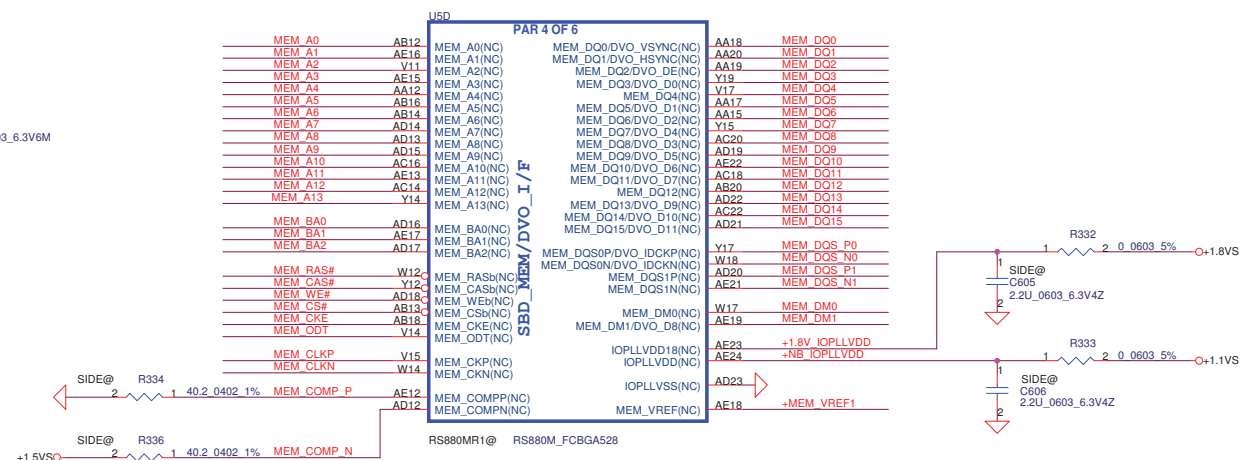
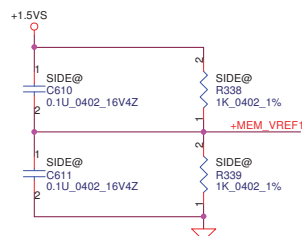


Strap pin

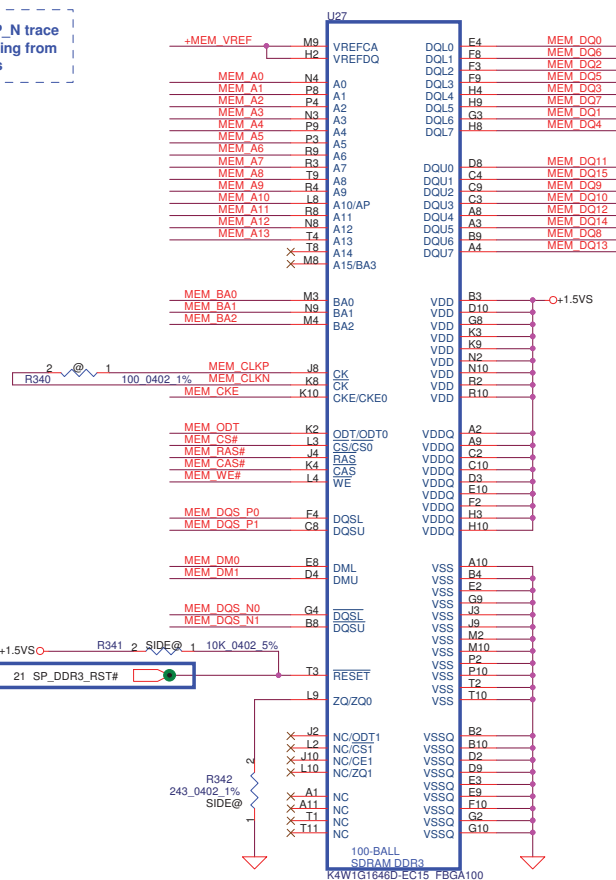
< HDMI hot-plug detection >

< Strap option pin or gate side-port memory IO >

Security Classification				Compal Secret Data				Title			
Issued Date				Deciphered Date				2008/04/14			
2008/04/14				2009/04/14				RS880M VEDIO/CLK GEN			
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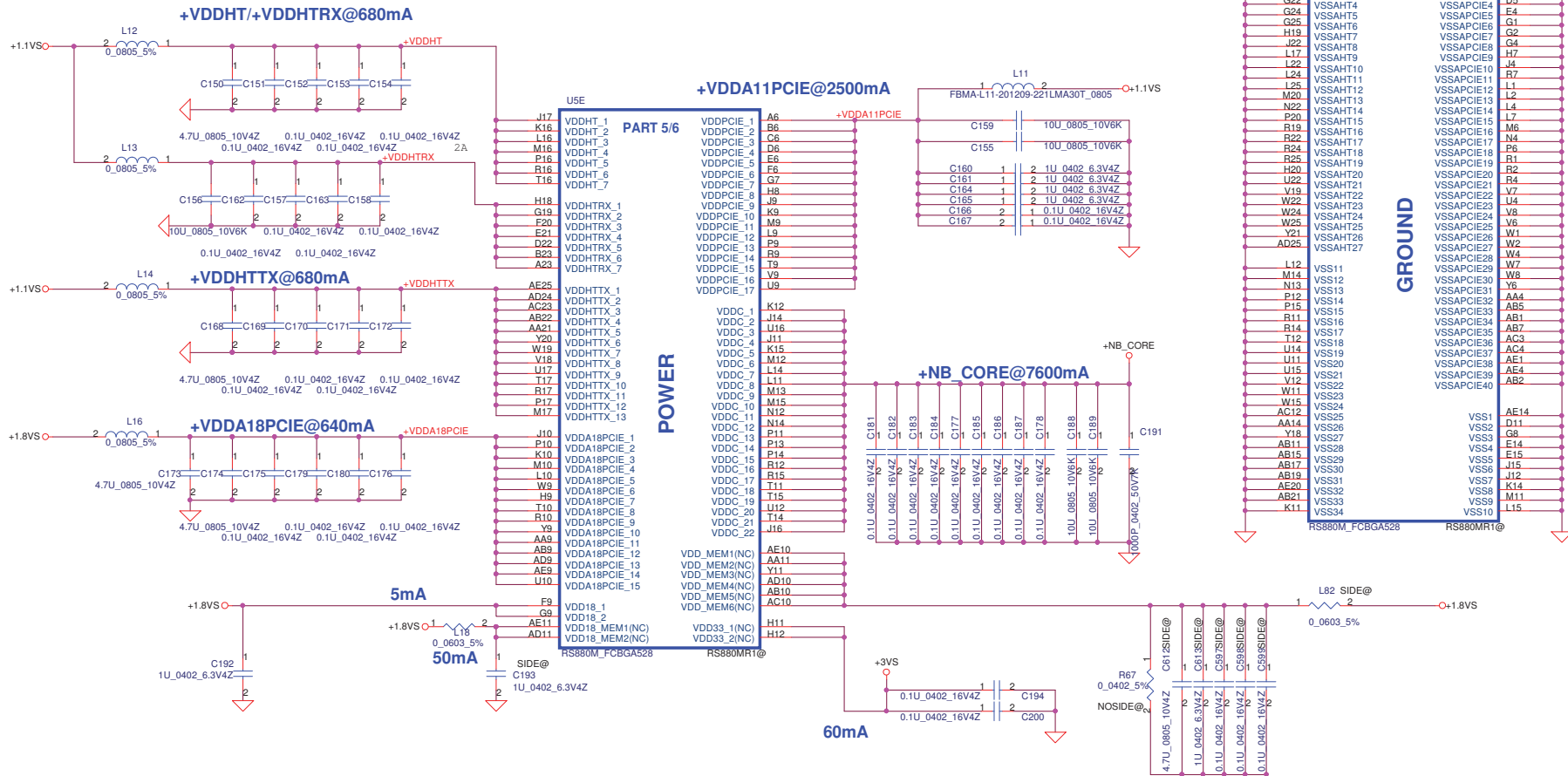
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions



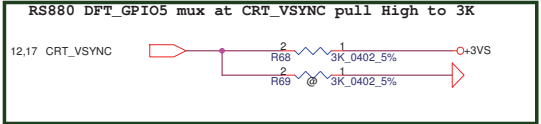
For Side port only



Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i> RS880M SIDE PORT		
Issued Date	2008/04/14	Deciphered Date	2009/04/14	Title		
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Security Classification	Compal Secret Data			Title	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	RS880MPWR/GND	
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DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

1 : Disable (RS880) ☐

0 : Enable (RS880)

PIN: RS880-->VSYNC#

RS780 use register to control PCI-E configure

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.

000 : 00001

001 : 00010

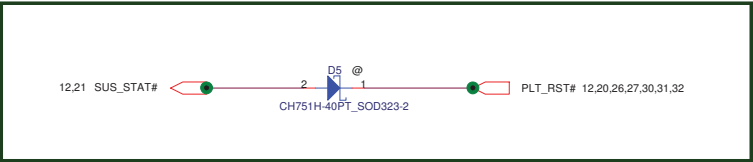
010 : 01011

011 : 00100

100 : 01010

101 : 01100

111 : 01011



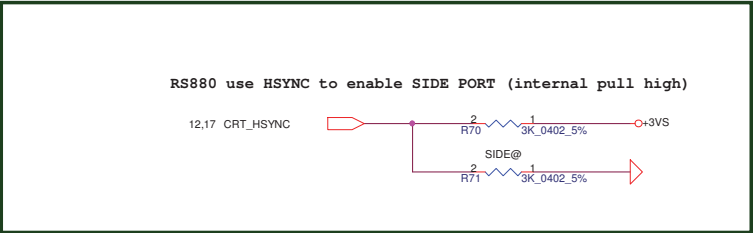
DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values

0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880:SUS_STAT#



DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

RX881: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)

0 : Enable

RS880: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS880) ☐

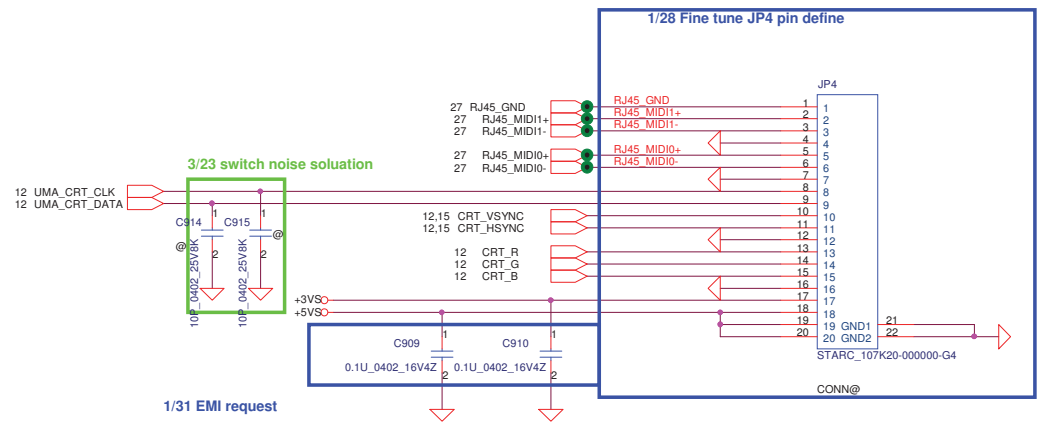
0 : Enable (RS880)

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Use SB820M internal clock gen

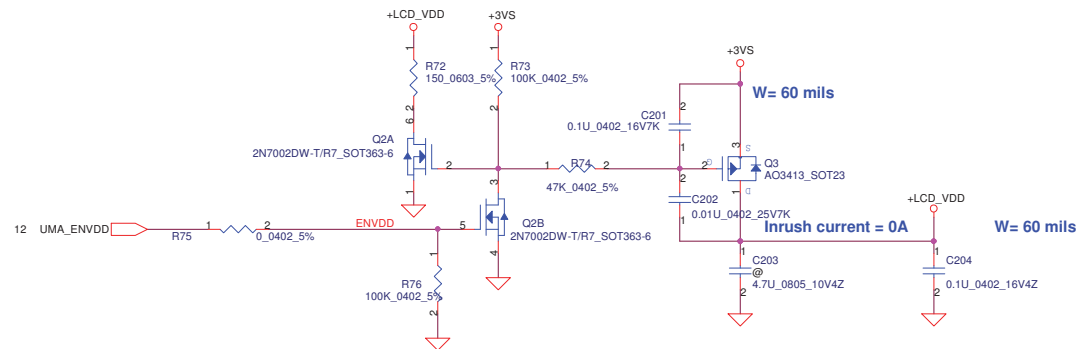
Security Classification		Compal Secret Data		Title	
Issued Date	2009-02-12	Deciphered Date	2009-02-12	CLOCK GENERATOR	
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				LA-6051P	1.0
Date: Tuesday, March 23, 2010				Sheet	16 of 45

CRT+RJ45 FFC conn
Pin=20pin, pitch=0.5

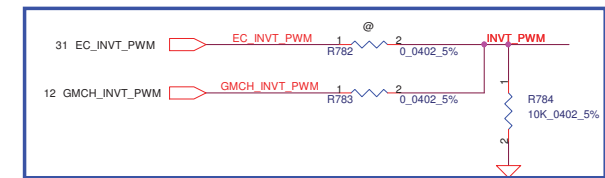
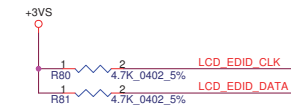
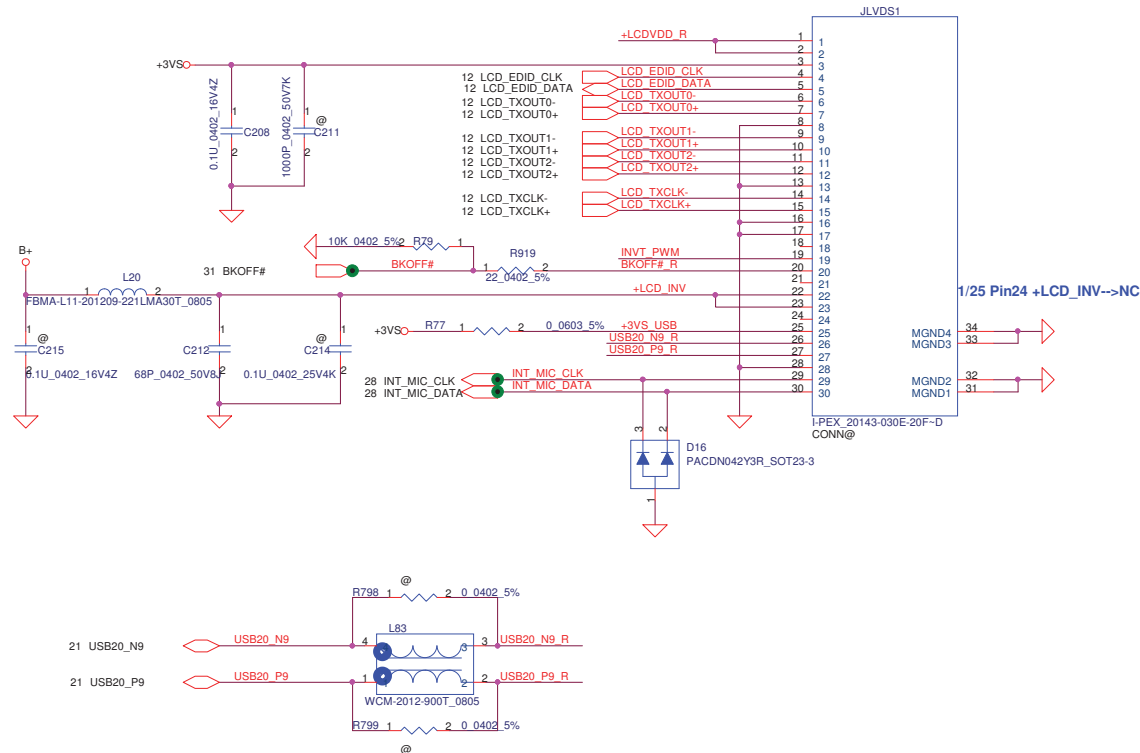


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Issued Date	2008/04/14	Deciphered Date	2009/04/14	Document Number		LA-6032P	
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				Rev	1.0		

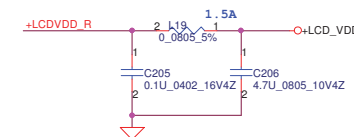
LCD/PANEL BD. Conn.



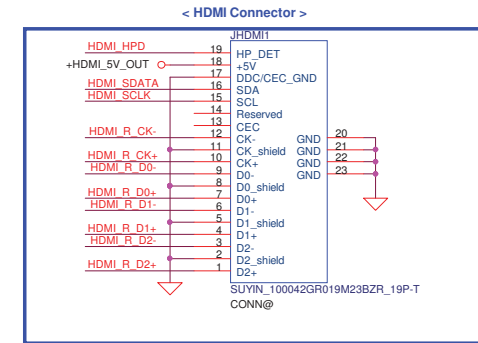
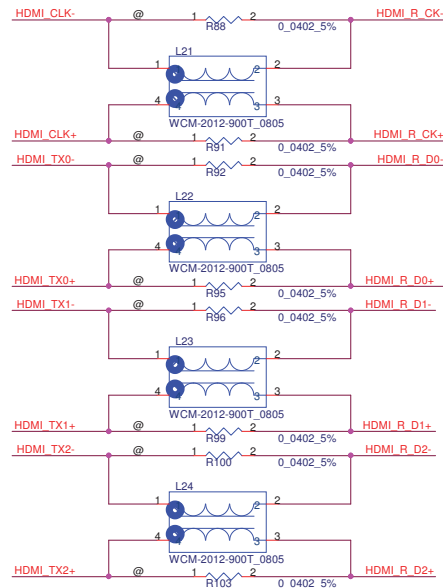
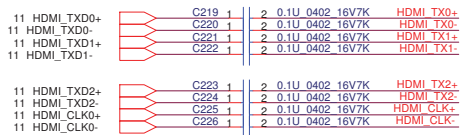
< LVDS Connector >



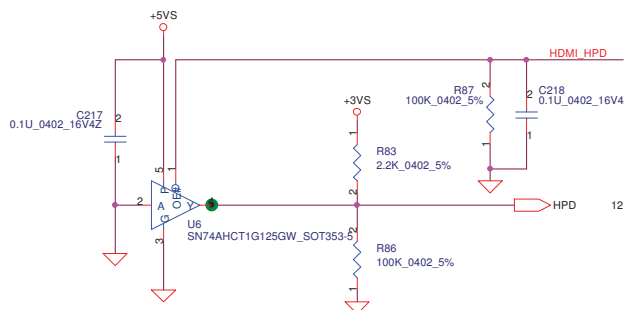
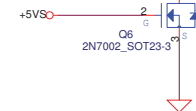
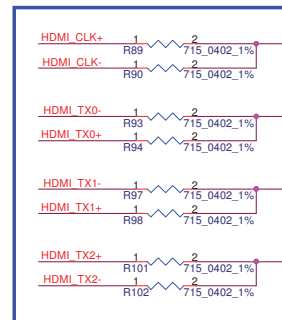
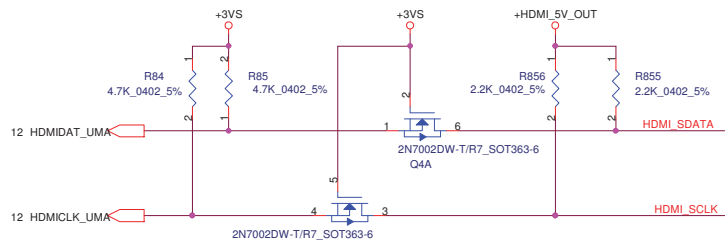
1/19 R782-->@ and R783/R784-->SMT for VB function



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					Document Number	LA-6032P	Rev	1.0
					Date:	Tuesday, March 23, 2010	Sheet	18

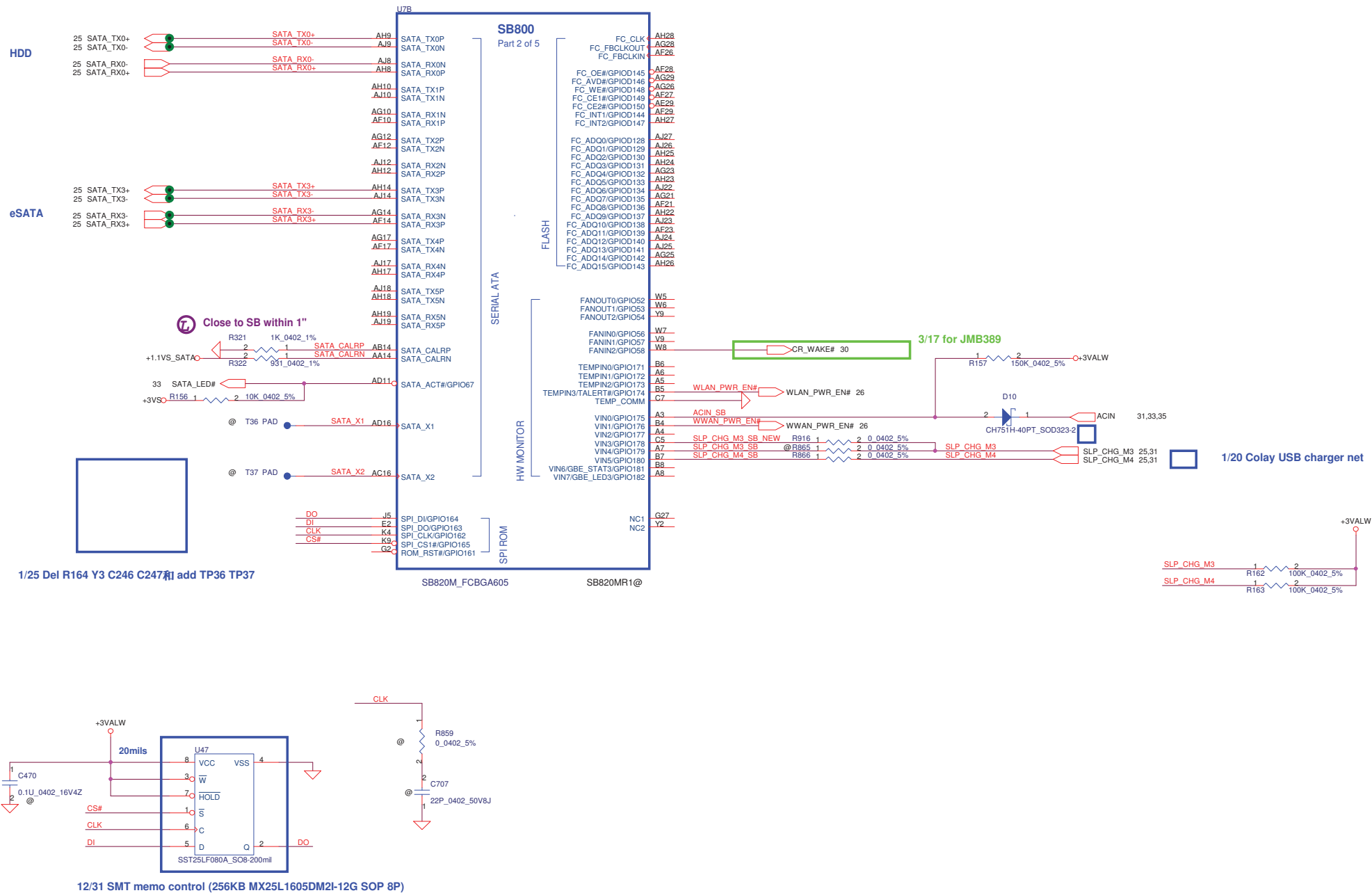


1/28 Update JHDMI1 footprint

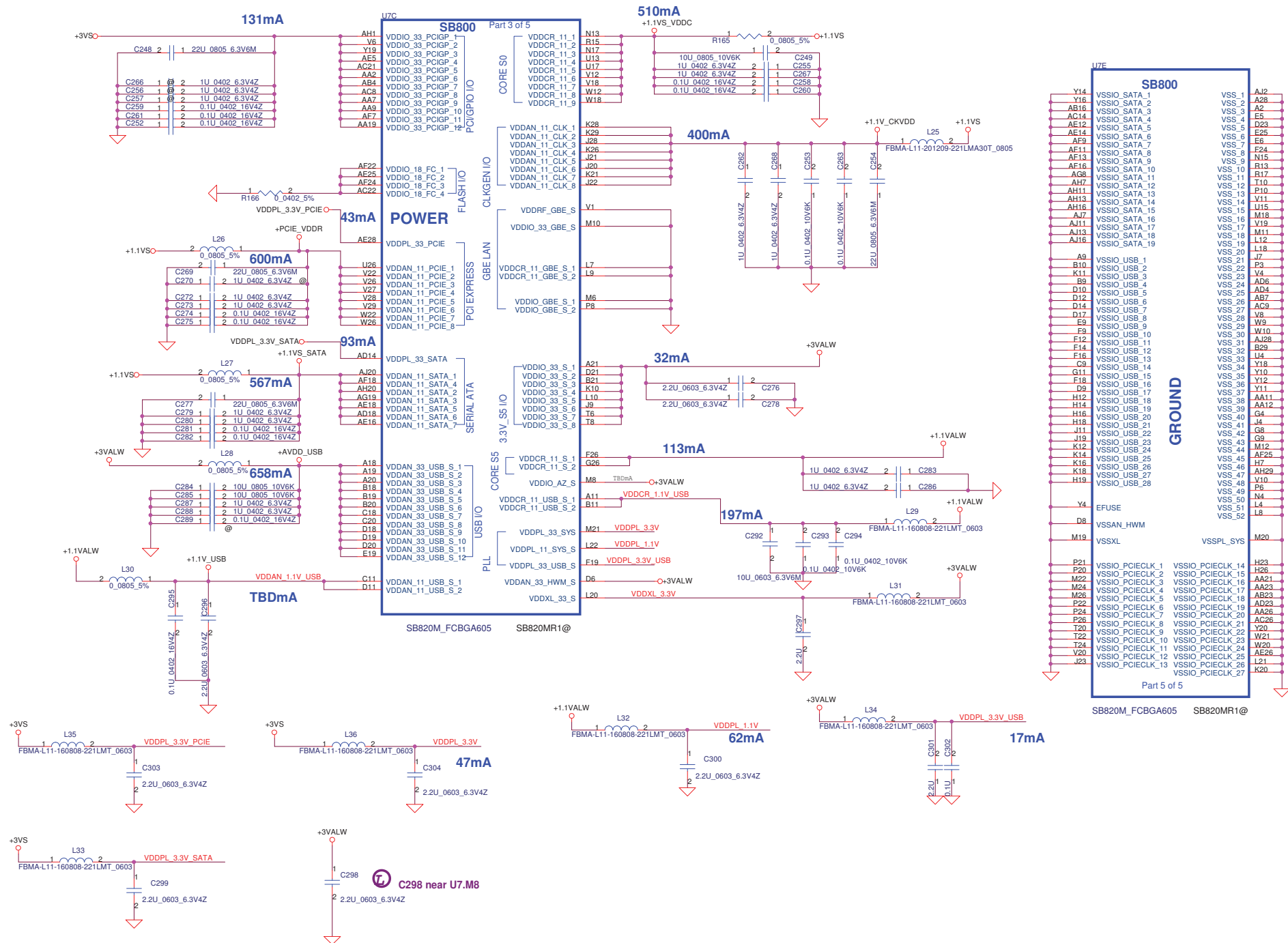


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HDMI/CEC				19 of 45
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				Document Number		LA-6032P	
				Date		Tuesday, March 23, 2010	
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				Revision		1.0	

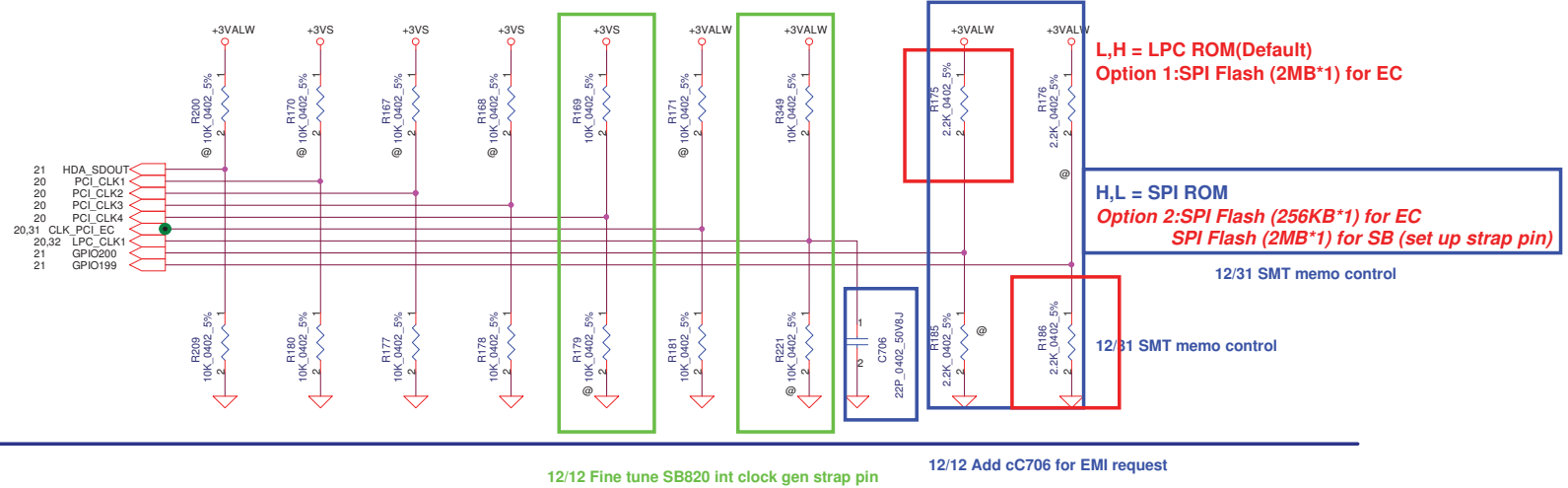


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Compal Electronics, Inc.				LA-6032P
SB820 Power/GND				Rev
Document Number				1.0
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REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1		GPIO200 (EC_PWM3)	GPIO199 (EC_PWM2)
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable DEFAULT	EC ENABLE	CLOCKGEN ENABLE DEFAULT		H,H = Reserved H,L = SPI ROM(Default)	
PULL LOW	Performance MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER DISABLE DEFAULT	IGNORE DEBUG STRAP DEFAULT	Inter CLK Gen Mode Disable	EC DISABLE DEFAULT	CLOCKGEN DISABLE		L,H = LPC ROM L,L = FWH ROM	



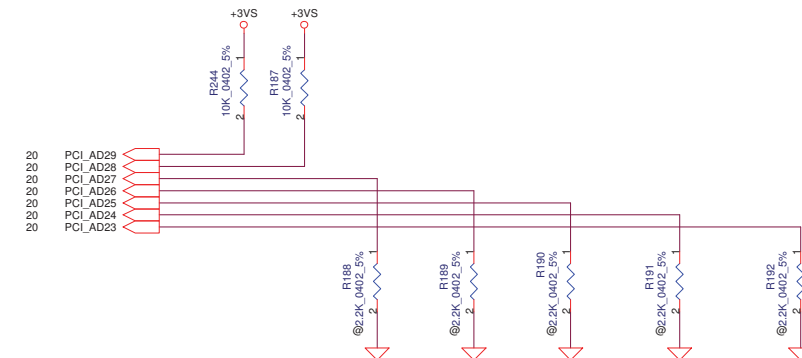
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

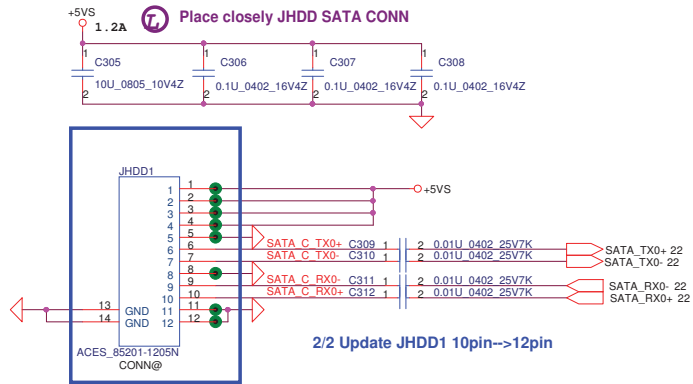
Check AD29,AD28 strap function

check default



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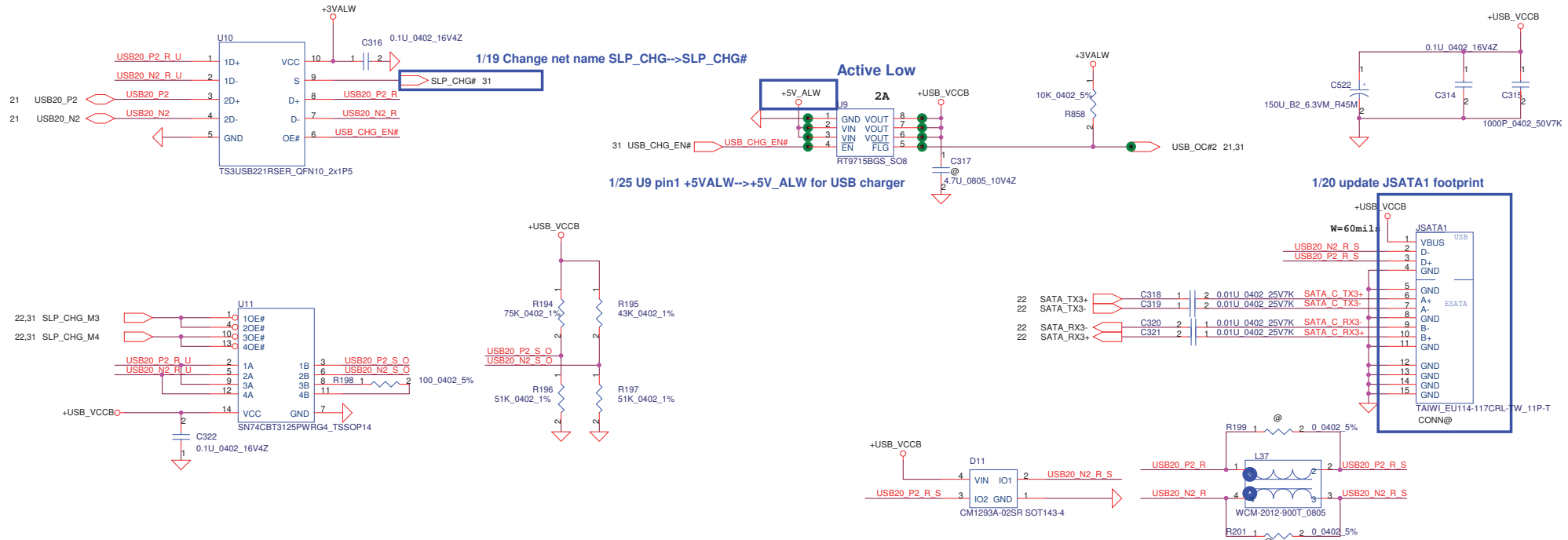
SATA transfer board



SATA FFC conn

Pin=12pin, pitch=1.0

E-SATA/USB



	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D

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Issued Date				2008/04/14				Deciphered Date			
								2009/04/14			
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				Document Number				LA-6032P			
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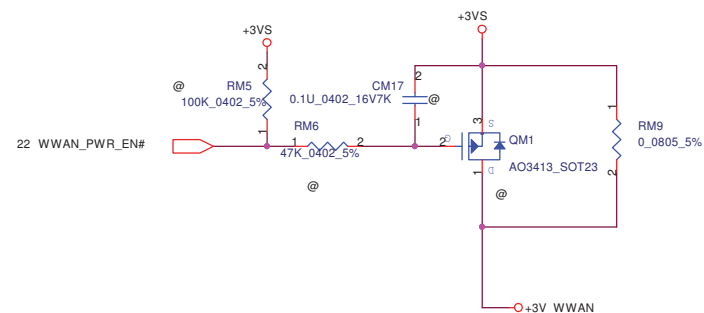
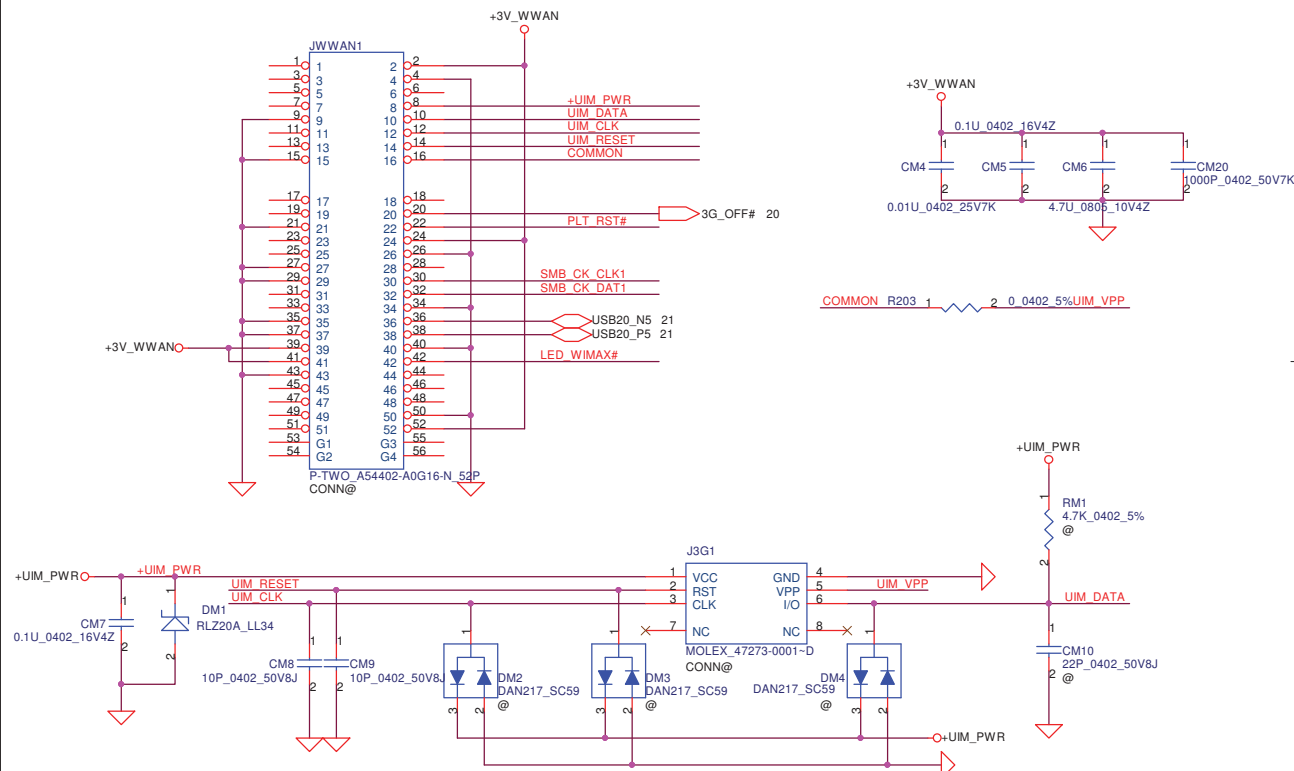
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SATA HDD/ODD

LA-6032P

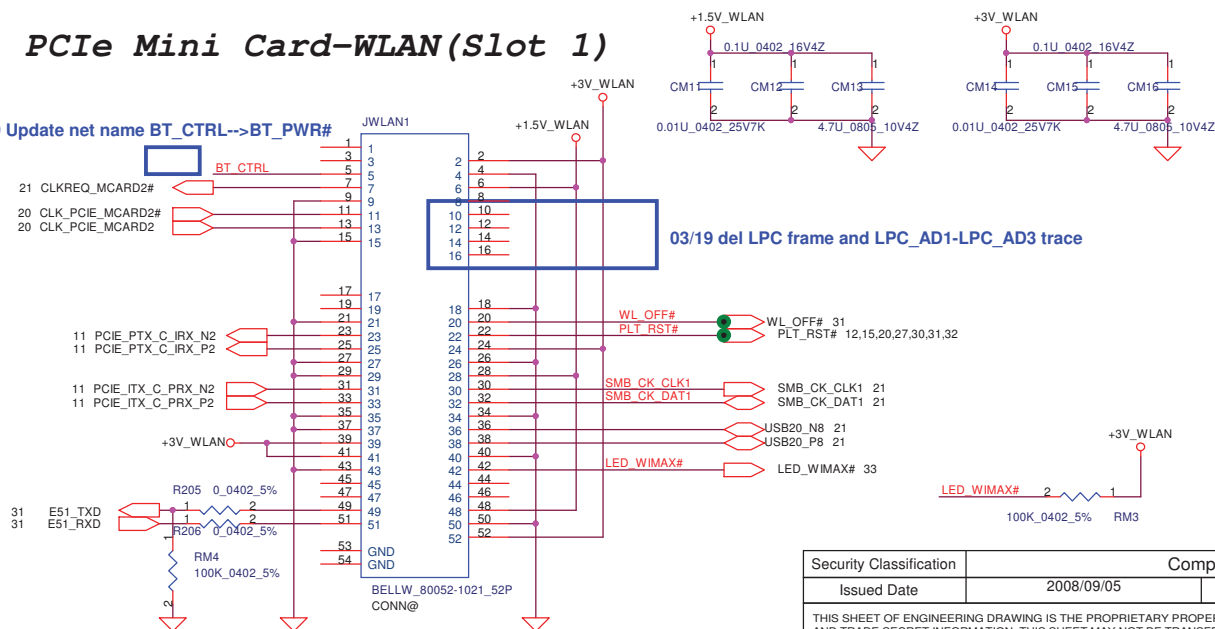
Rev 1.0

PCIE Mini Card-3G/WWAN (Slot 2)



PCIe Mini Card-WLAN(Slot 1)

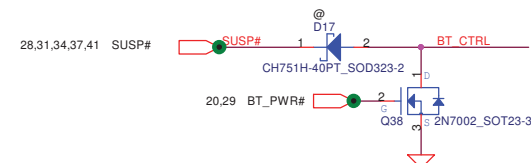
01/19 Update net name BT_CTRL-->BT_PWR#



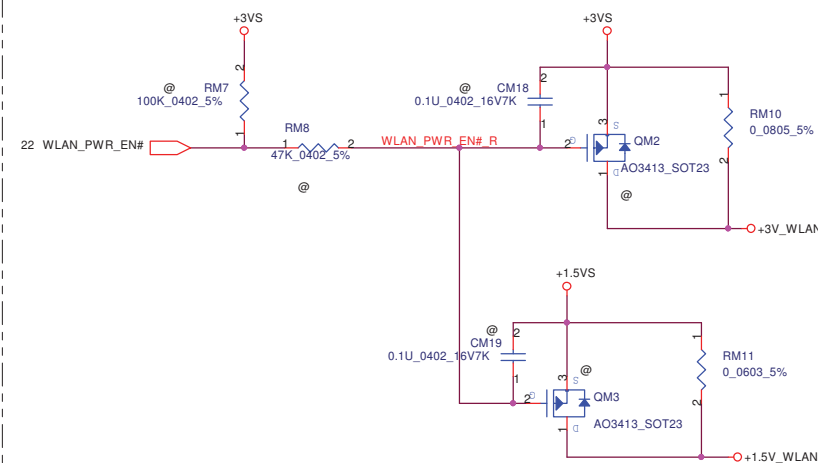
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

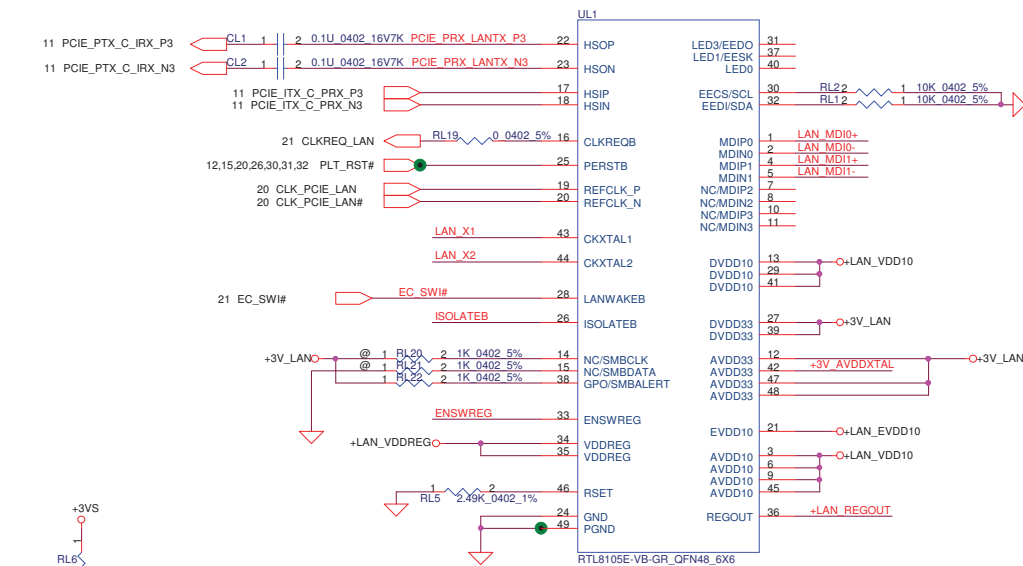
****If +3V_WLAN is +3VS, please remove D17.**



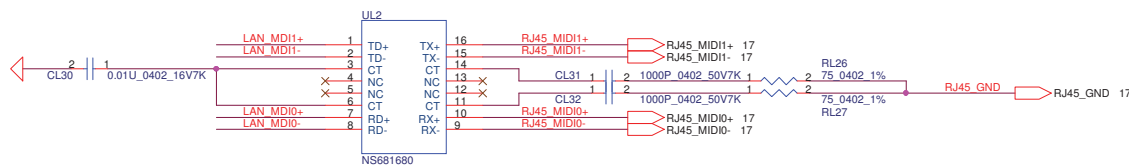
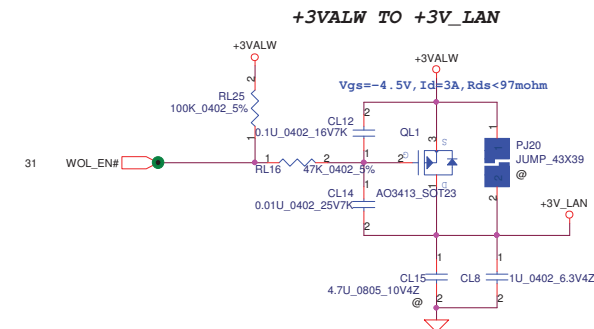
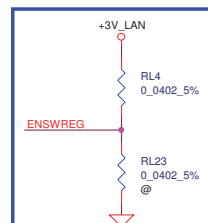
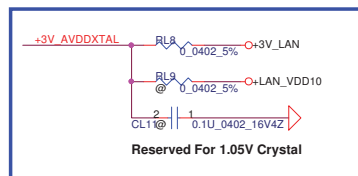
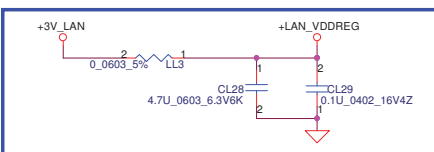
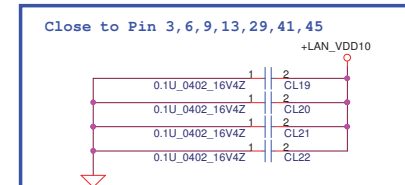
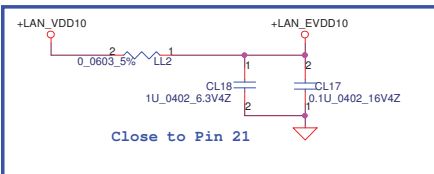
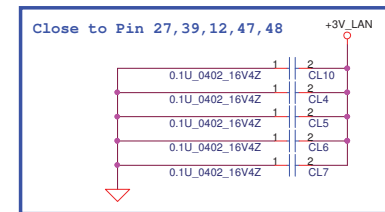
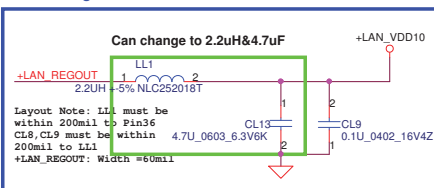
01/21 Add D17 and Q38 for BT control



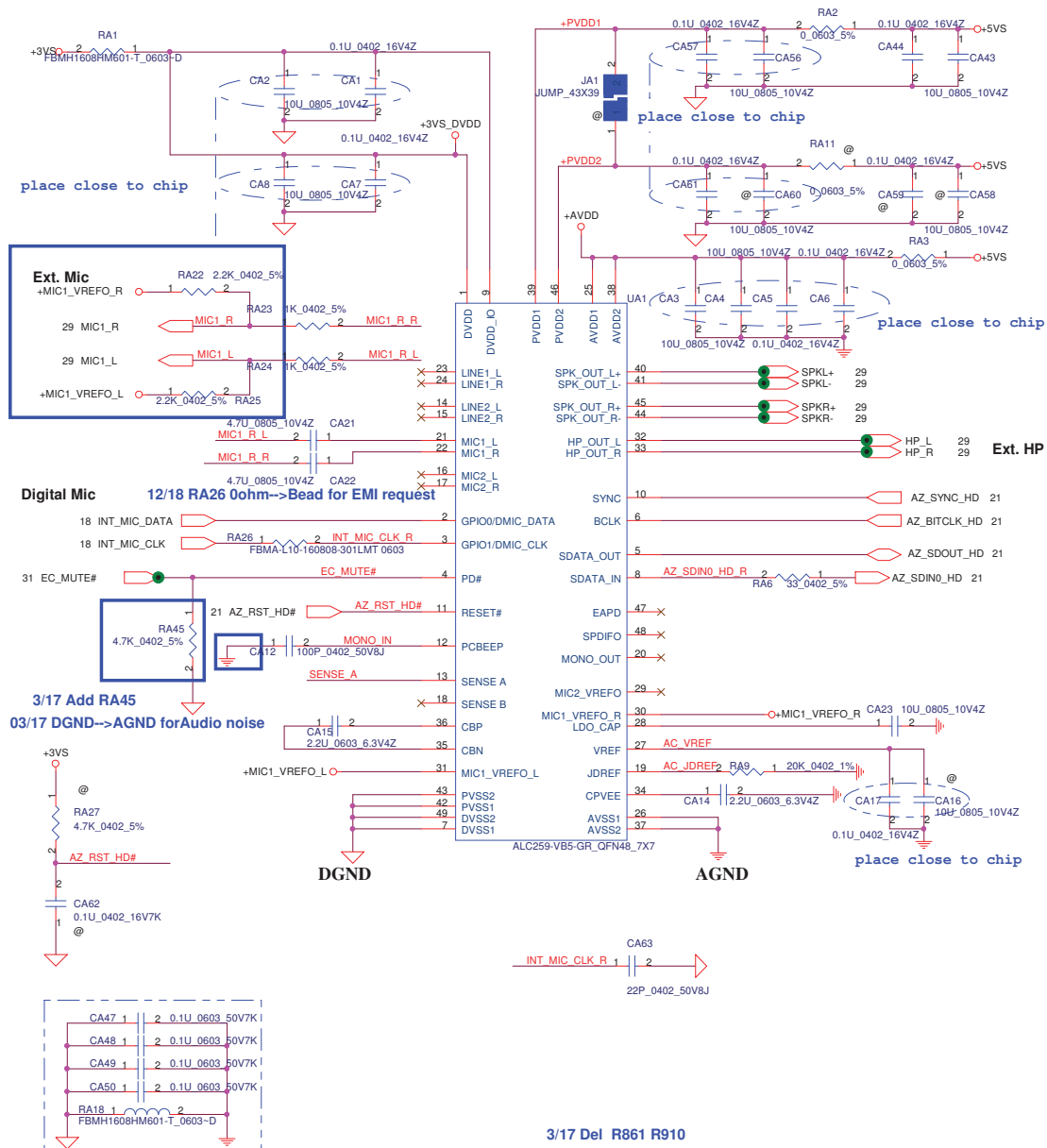
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Issued Date	2008/09/05	Deciphered Date	2009/09/05	Title PCle-WLAN/HDDVD/NAND/NEW			
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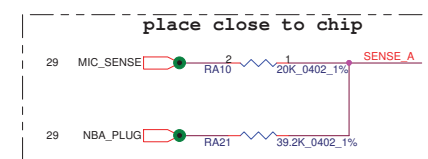
3/10 Change CL13 0805-->0603



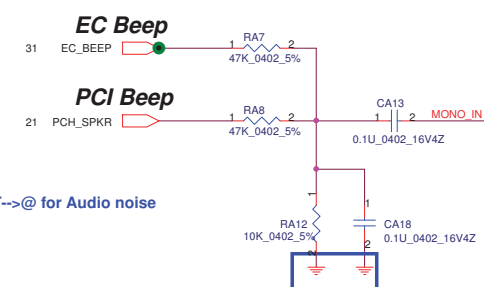
Security Classification		Compal Secret Data		Title	
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Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

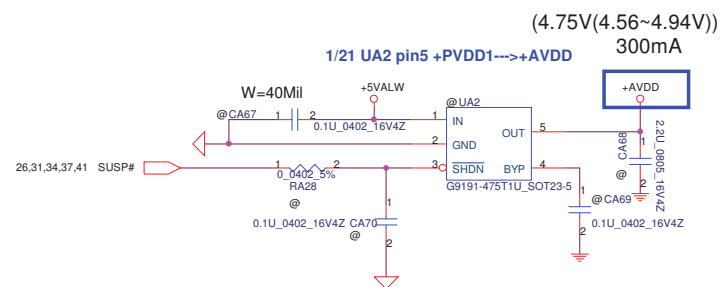


Beep sound



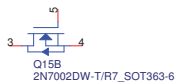
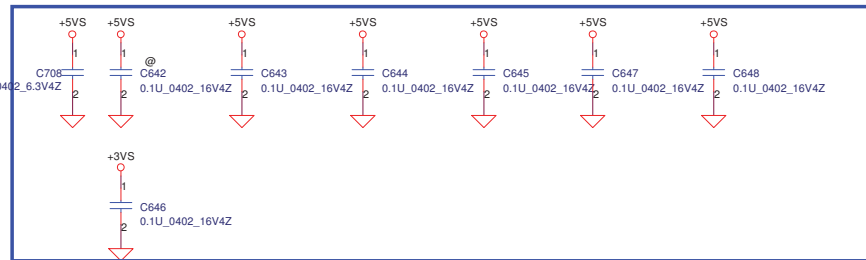
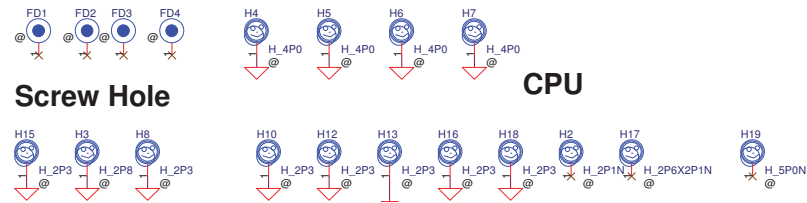
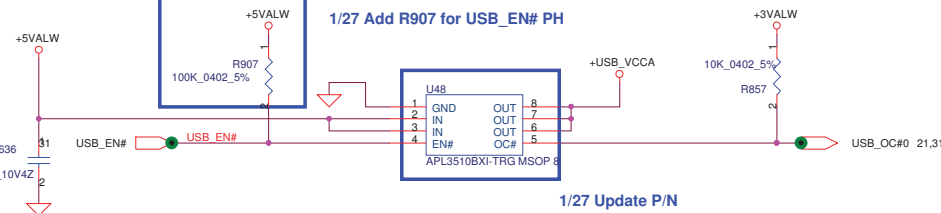
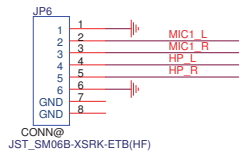
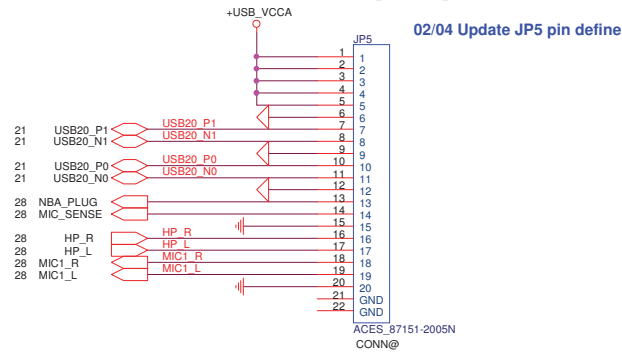
03/12 CA15 SMT-->@ for Audio noise

03/17 DGND-->AGND for Audio noise

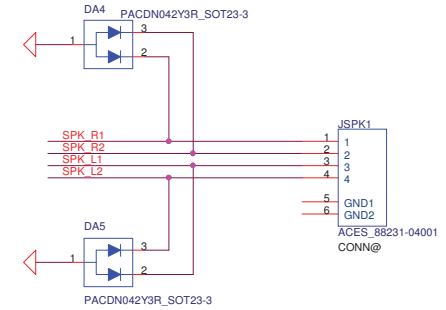
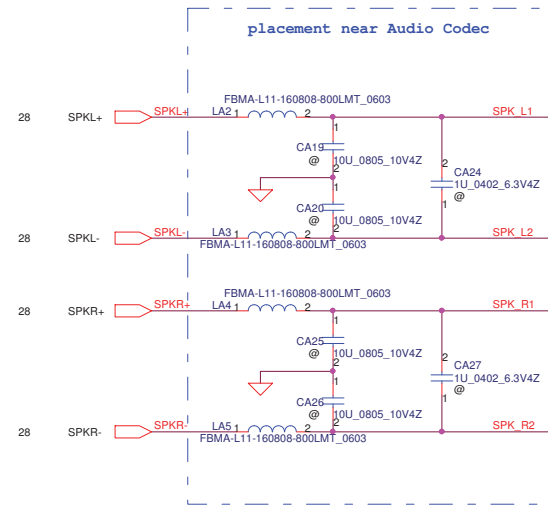


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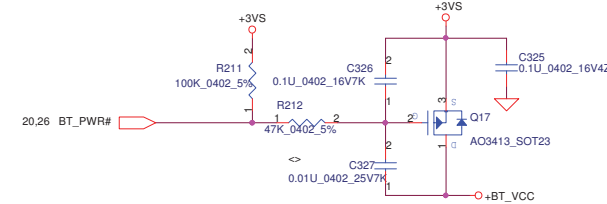
USB+Audio FFC conn Pin=20pin, pitch=0.5



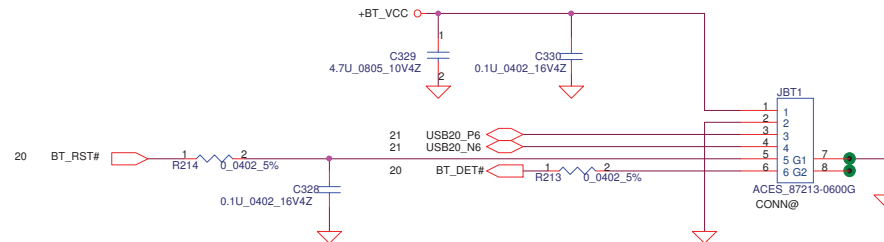
Speaker Connector



BlueTooth Interface



(MAX=200mA)



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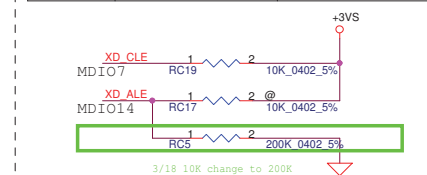
AMP/Audio Jack/HP/SPEAKER/VR

LA-6032P

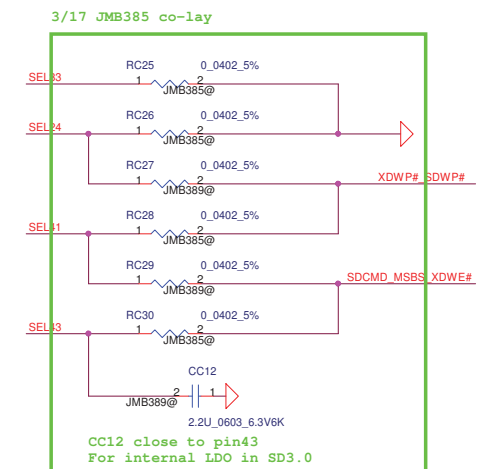
Rev 1.0

[illegible]

Pin name	Description	
	High	low
MDIO14	on board ★	add-in card
MDIO14	CR_LED high active	CR_LED low active★



Place RC5, RC17, RC19 close to pin42

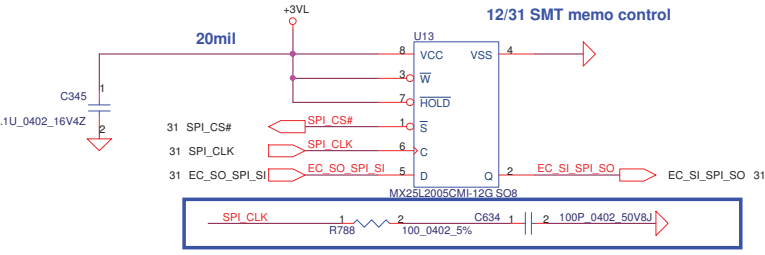


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Title	

Size	Document Number	Rev
Custom		0

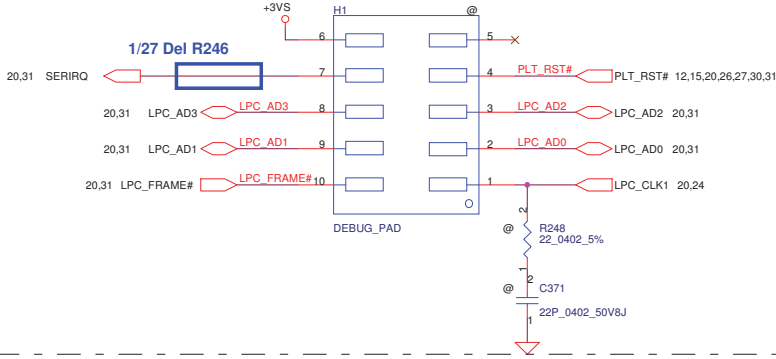
Option 1:SPI Flash (2MB*1) for EC
Option 2:SPI Flash (256KB*1) for EC
SPI Flash (2MB*1) for SB (set up strap pin)

SPI Socket: SP07000F500 & SP07000H900
2MB P/N:MXIC SA00002TO00 S IC FL 16M MX25L1605DM2I-12G SOP 8P ROM
256KB P/N:MXIC SA00003GK00 S IC FL 2M MX25L2005CMI-12G SOP 8P

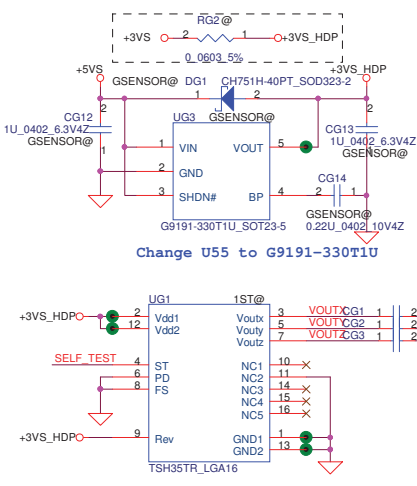


12/18 <BOM>R788 @-->100ohm and C634 @-->100P for RF request

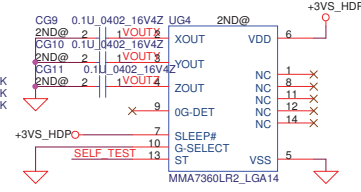
LPC Debug Port (Please place the PAD under DDR DIMM)



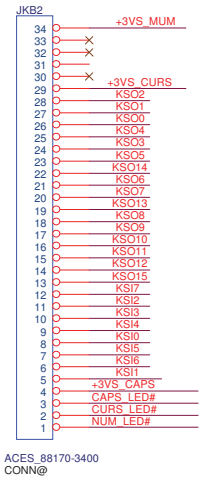
G-Sensor



Reserve Freescale

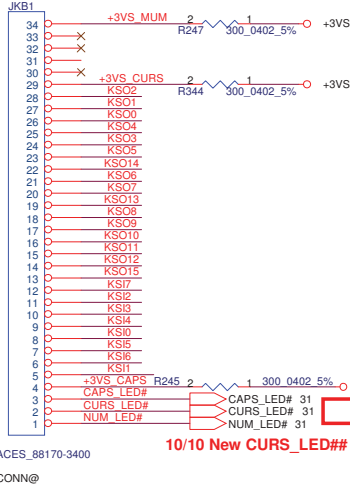


11.6 KEYBOARD CONN.



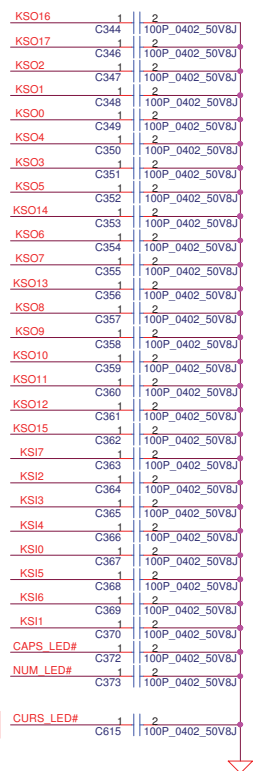
New keyboard

13.3 KEYBOARD CONN.



10/10 New CURS_LED## for 11.3&13.6

10/10 New CURS_LED# cap for 11.3&13.6

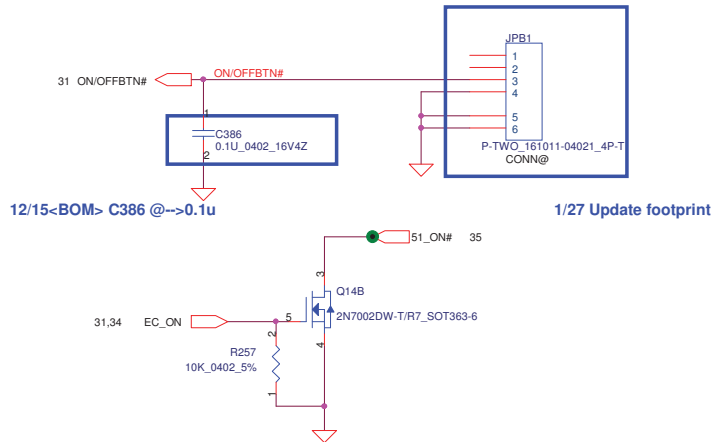


CURS_LED#

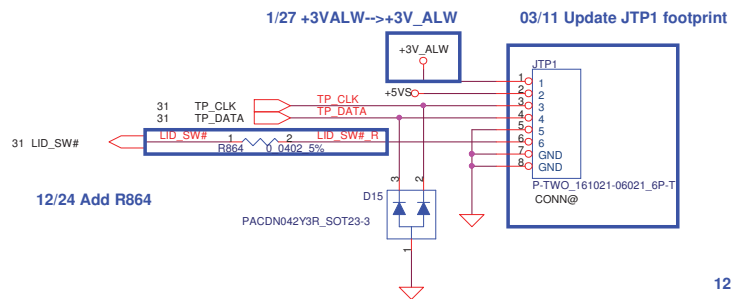
03/11 update G-sensor P/N

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Power Button & Lid switch



Touch/B Connector



03/10 Fine tune R813 R815 120ohm-->220ohm



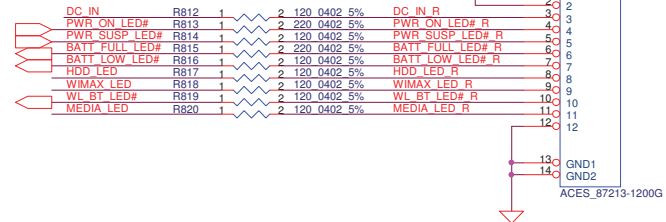
31 PWR_ON_LED#

31 PWR_SUSP_LED#

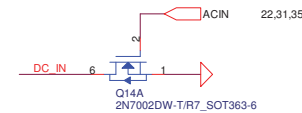
31 BATT_FULL_LED#

31 BATT_LOW_LED#

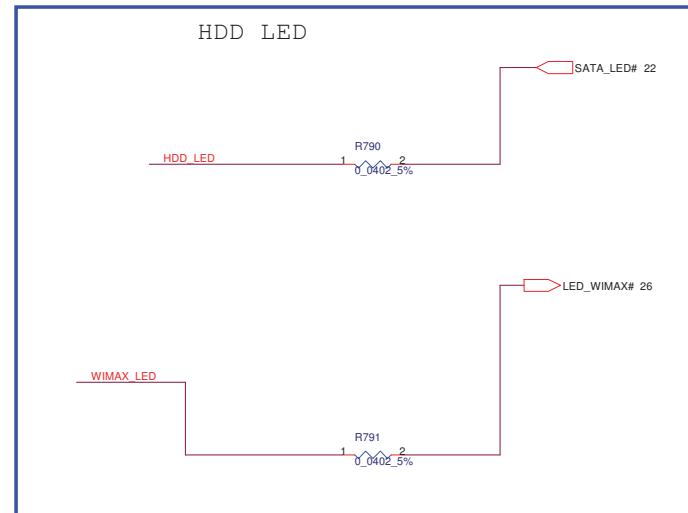
31 WL_BT_LED#



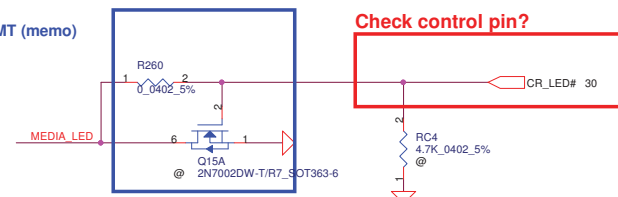
DC-IN LED



HDD LED



03/10 Q15-->@ and R260 @-->SMT (memo)



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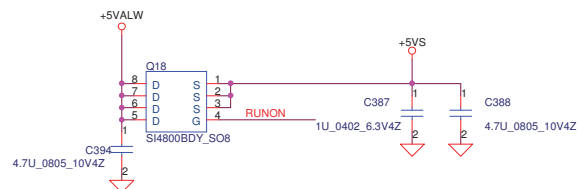
LED/LID/PB/FB/SCREW HOLE

LA-6032P

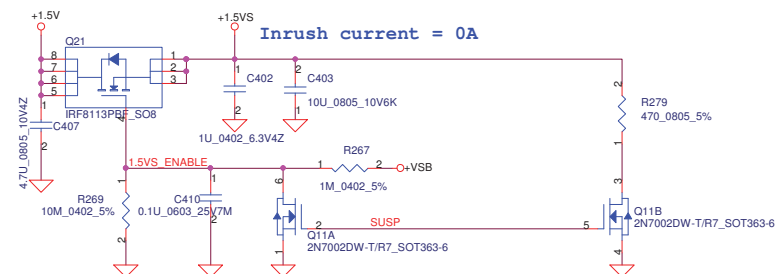
Rev 1.0

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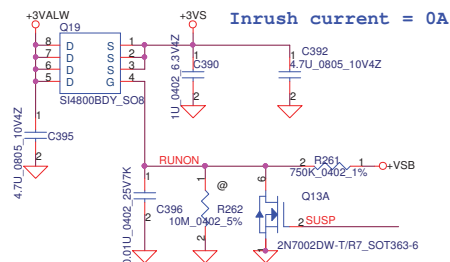
< +5VALW TO +5VS >



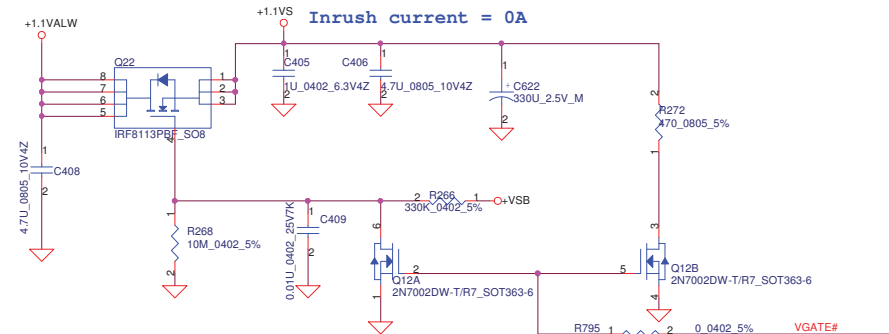
< +1.5V TO +1.5VS >



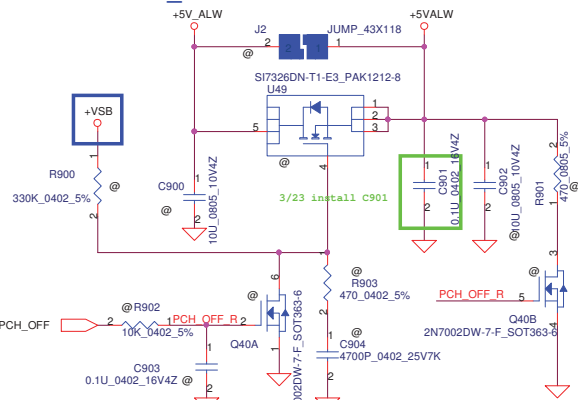
< +3VALW TO +3VS >



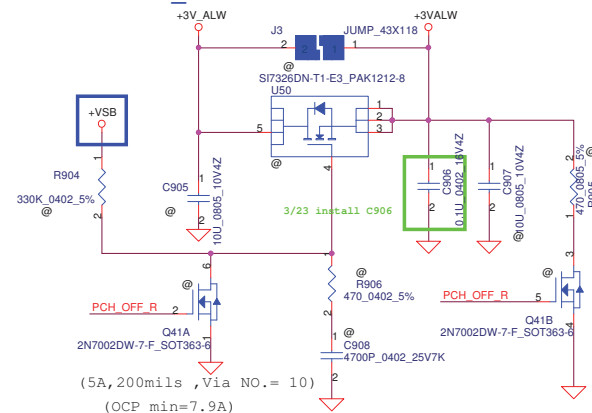
< +1.1VALW TO +1.1VS >



+5V_ALW to +5VALW Transfer

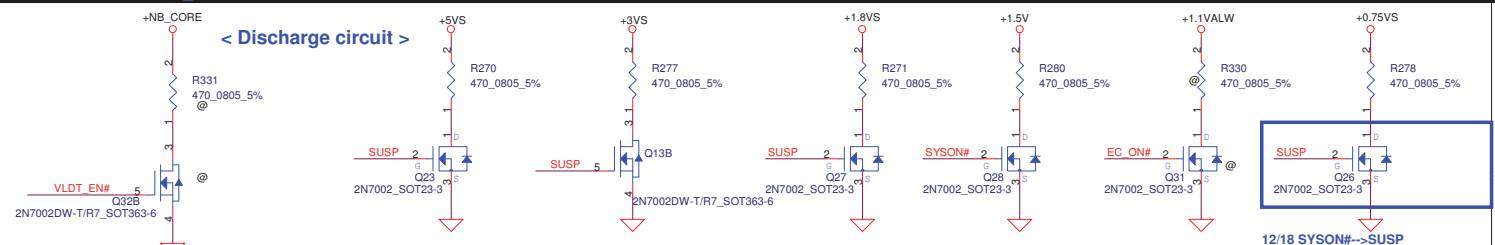
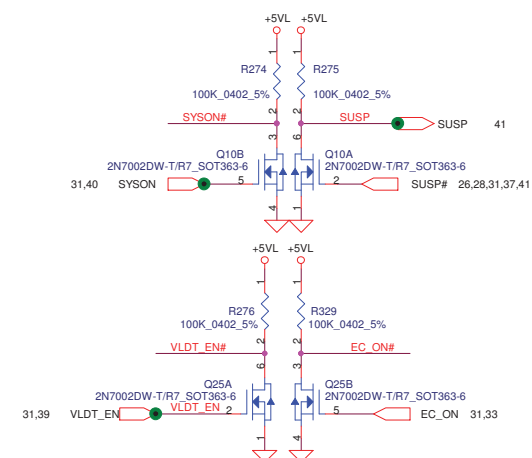


+3V_ALW to +3VALW Transfer



1/25 Add +5V_ALW to +5VALW Transfer
+3V_ALW to +3VALW Transfer

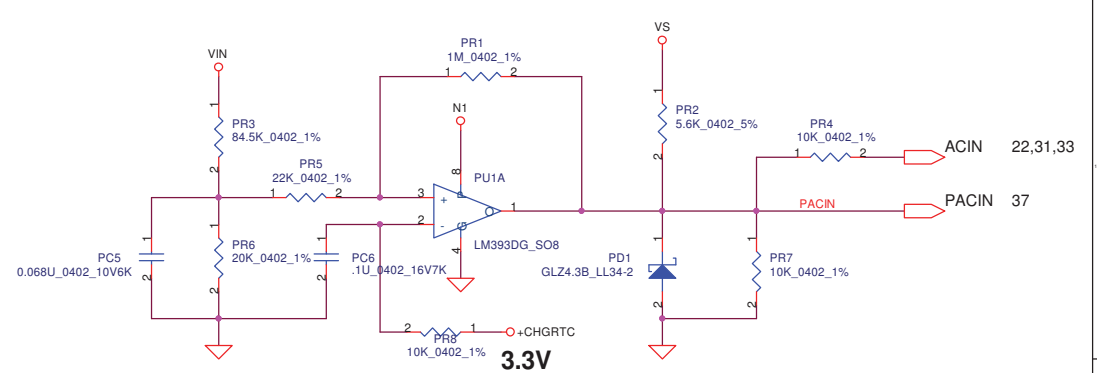
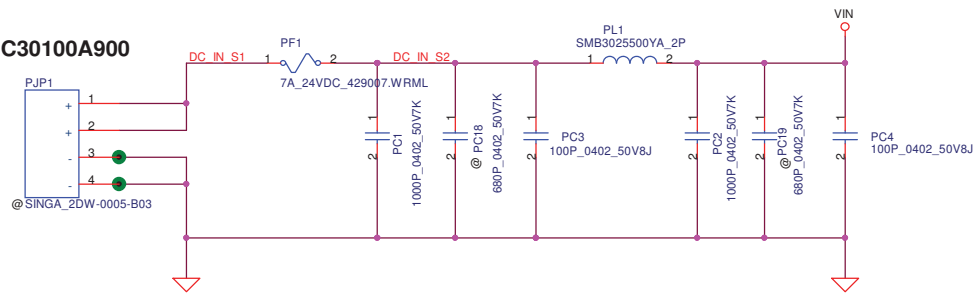
< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >



12/18 SYSON#-->SUSP

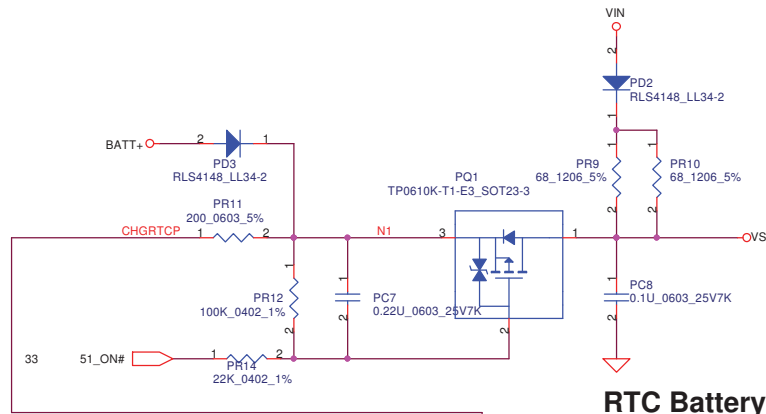
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Issued Date	2008/04/14	Deciphered Date	2009/04/14	Title	DC/DC Circuits	
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DC30100A900

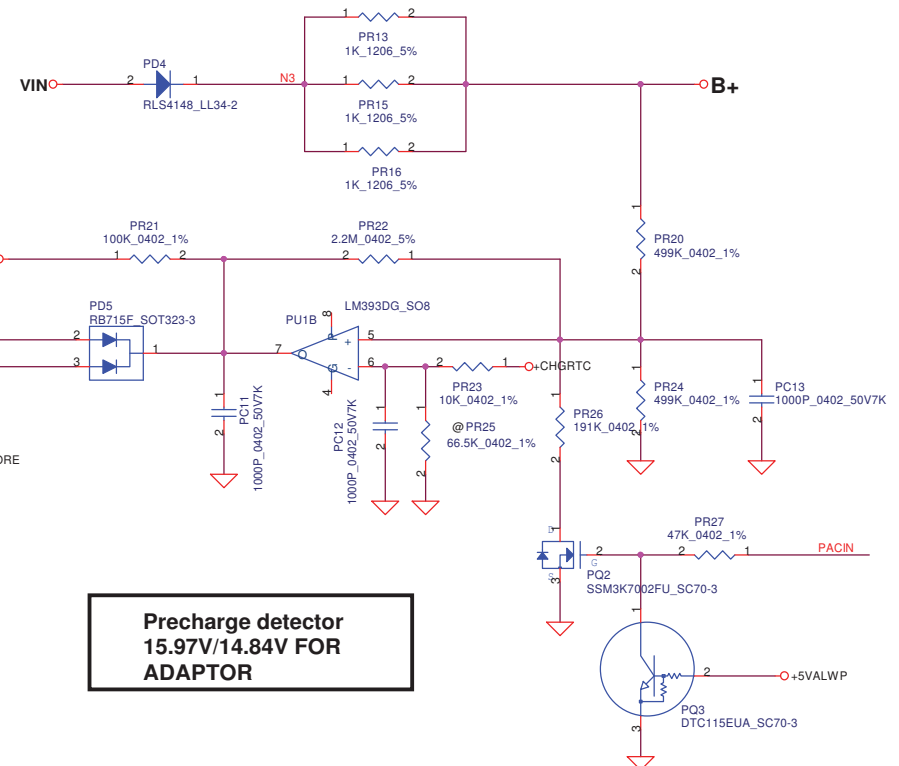
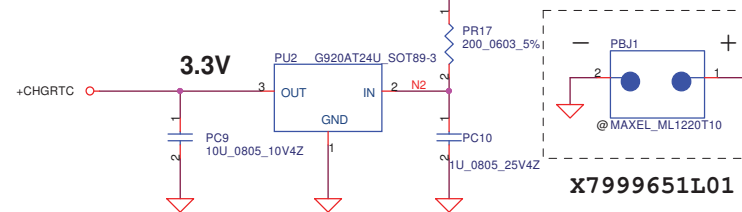


Vin Detector

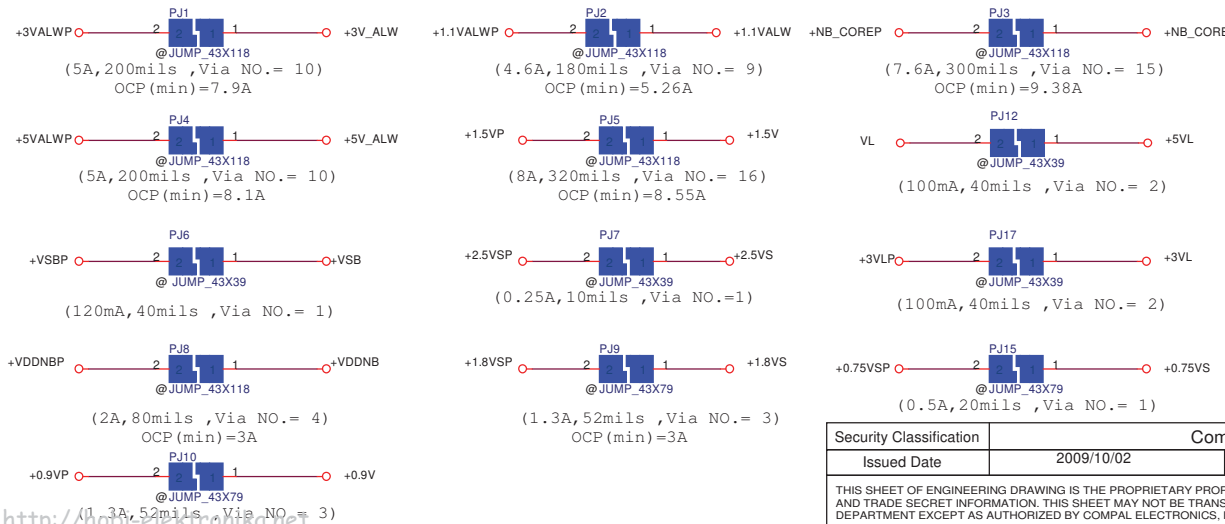
High 18.384 17.901 17.430
 Low 17.728 17.257 16.976



RTC Battery

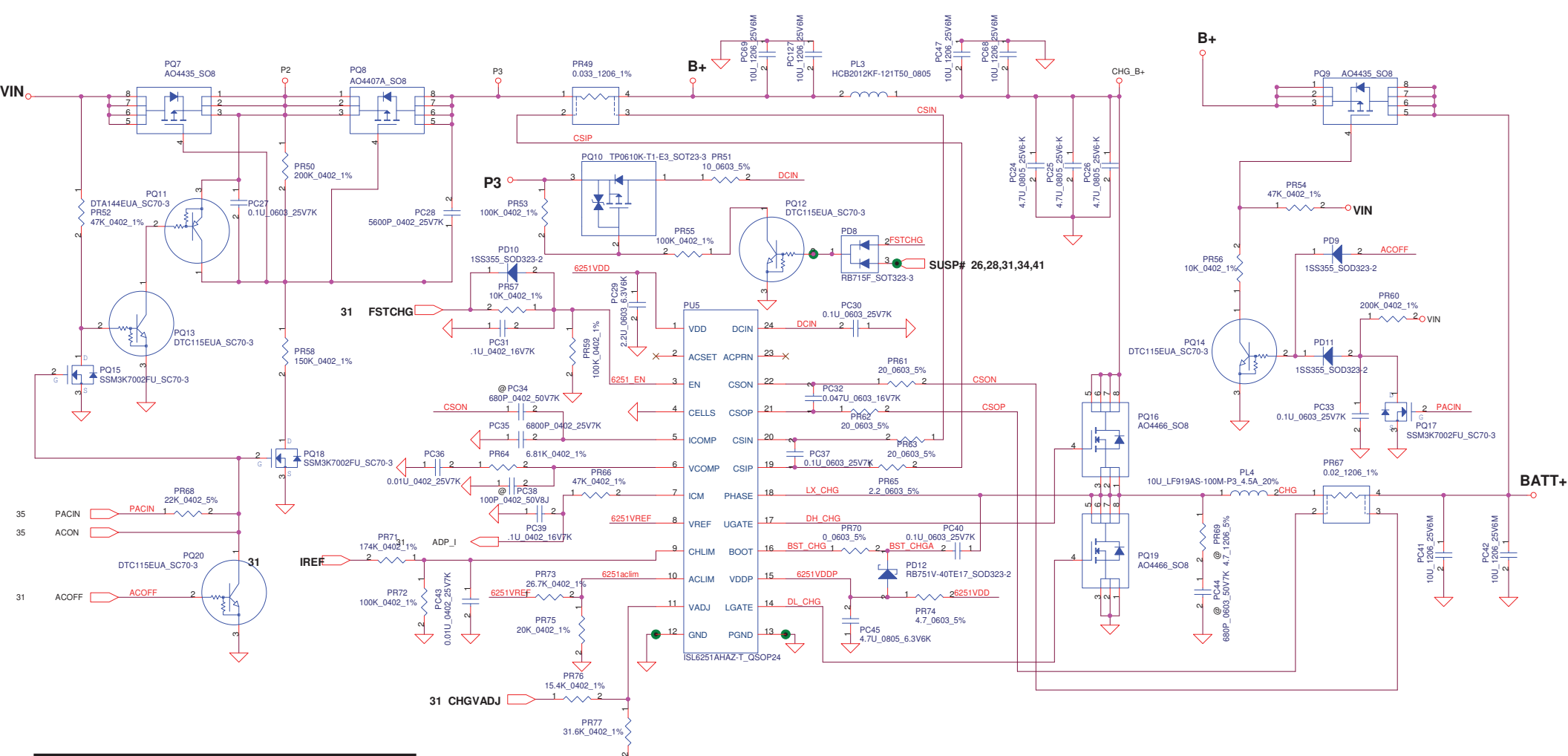


Precharge detector 15.97V/14.84V FOR ADAPTOR



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DCIN/DECTOR			
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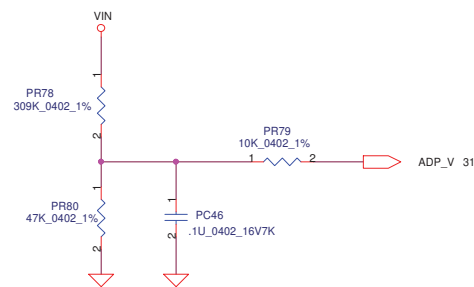


Iadapater=0~2.368A (45W) CP=Iadapater*0.92 CP=2.178A

CC=0.25A~3A
IREF=1.096*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

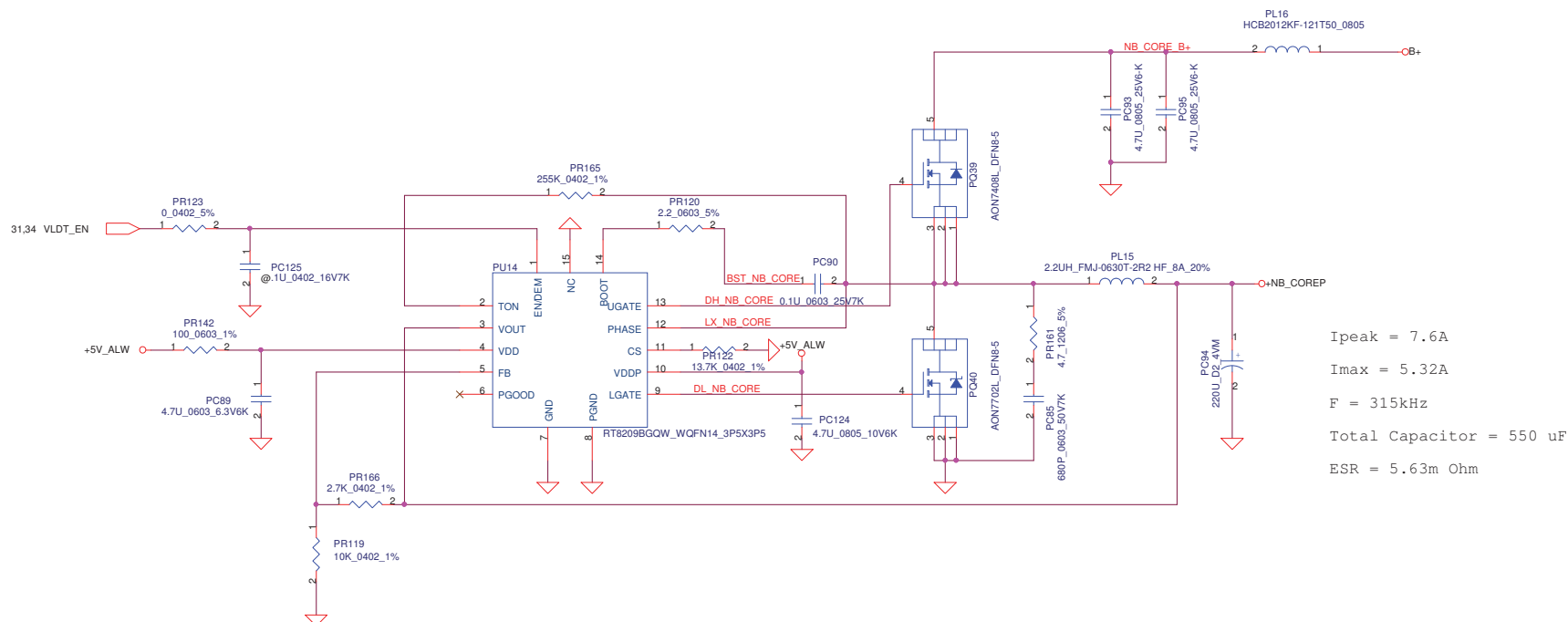
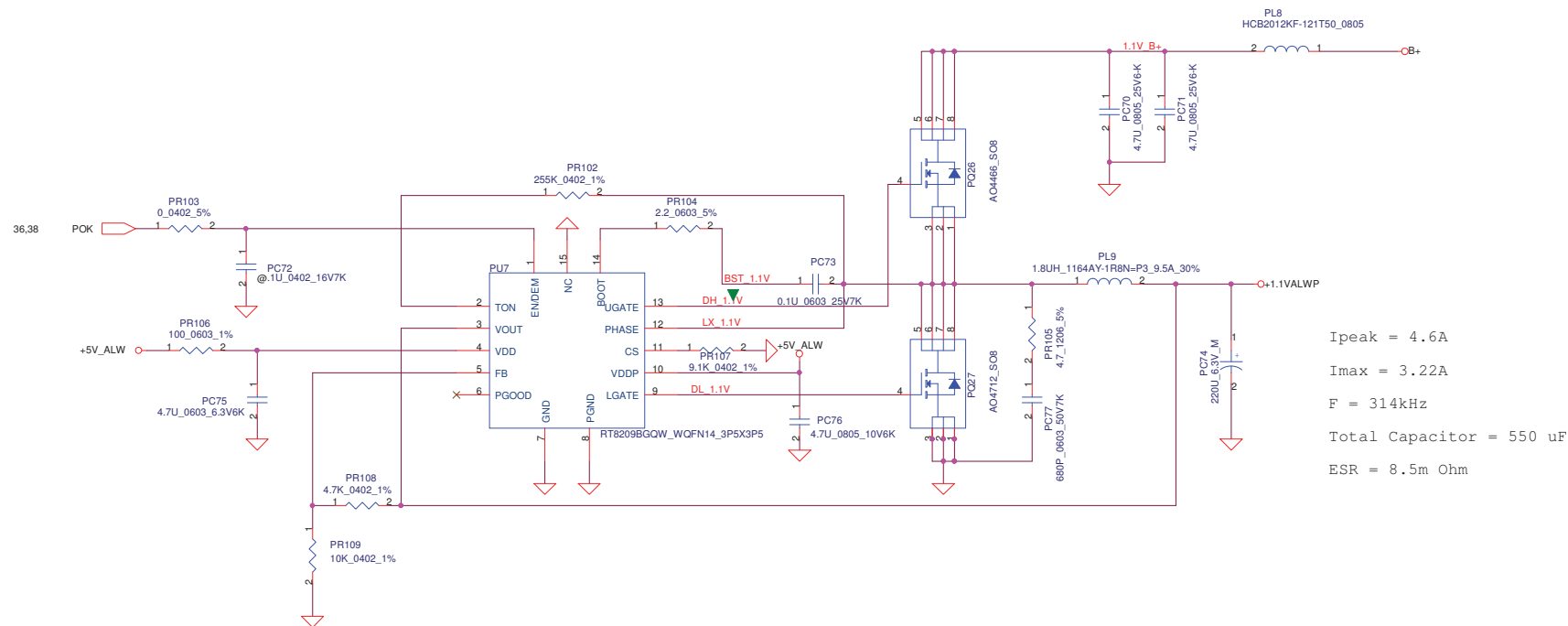
CP mode
Vaclm=2.39*(20K/(152K/(20K/(152K+26.7K/(152K)))=1.04596V
Iinput=(1/0.02)*((0.05*Vaclm)/(2.39+0.05))
where Vaclm=1.04596V, Iinput=2.178A



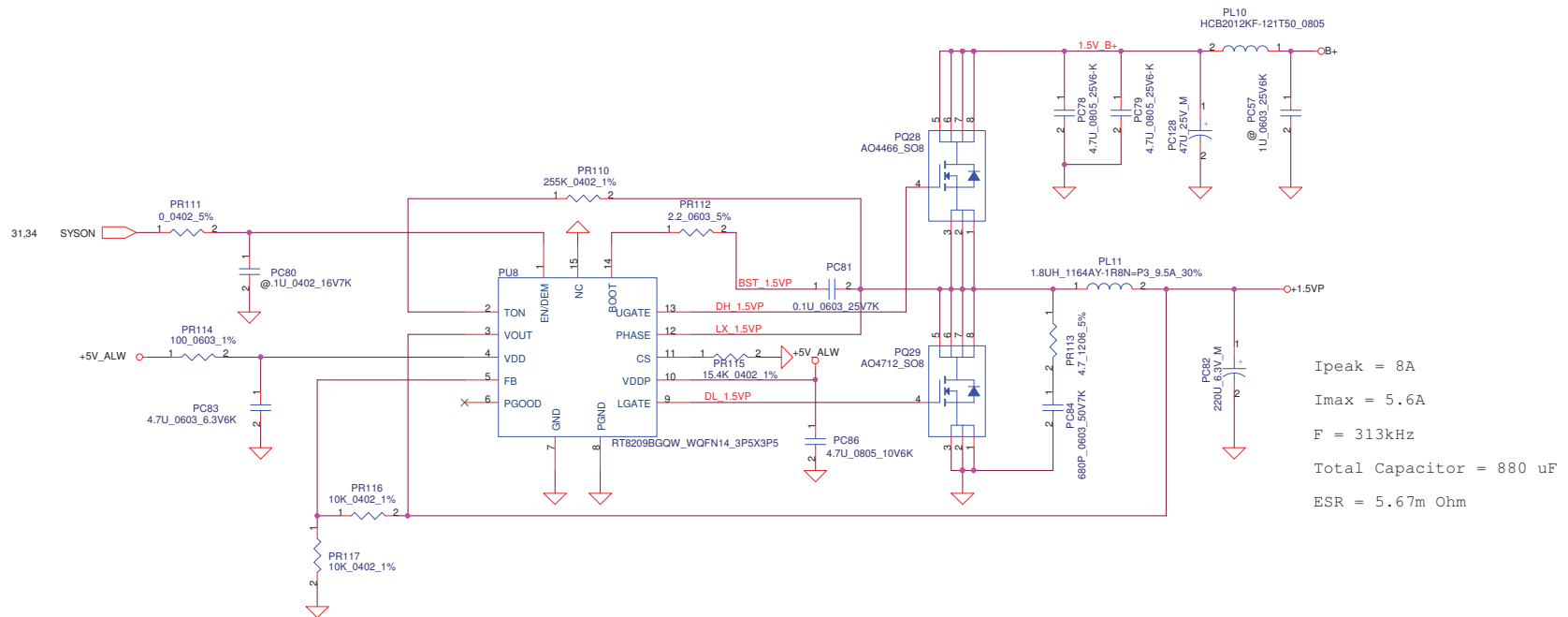
Ipeak = 5A
 Imax = 3.5A
 F = 305kHz
 Total Capacitor = 150 uF
 ESR = 18m Ohm

Ipeak = 5A
 Imax = 3.5A
 F = 245kHz
 Total Capacitor = 150 uF
 ESR = 18m Ohm

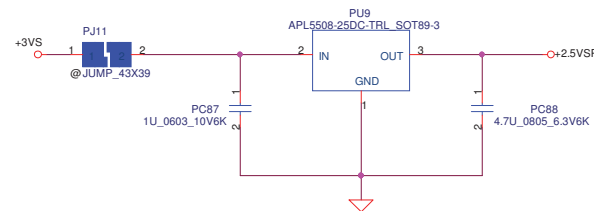
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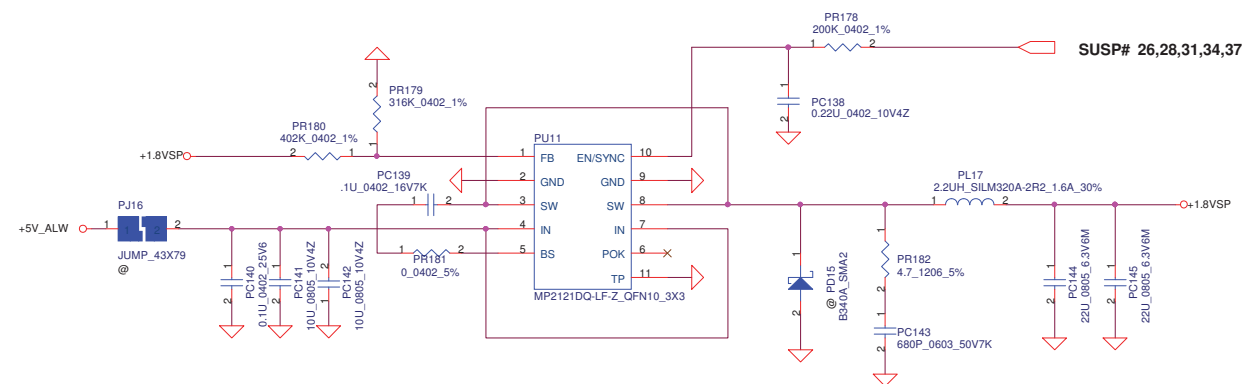
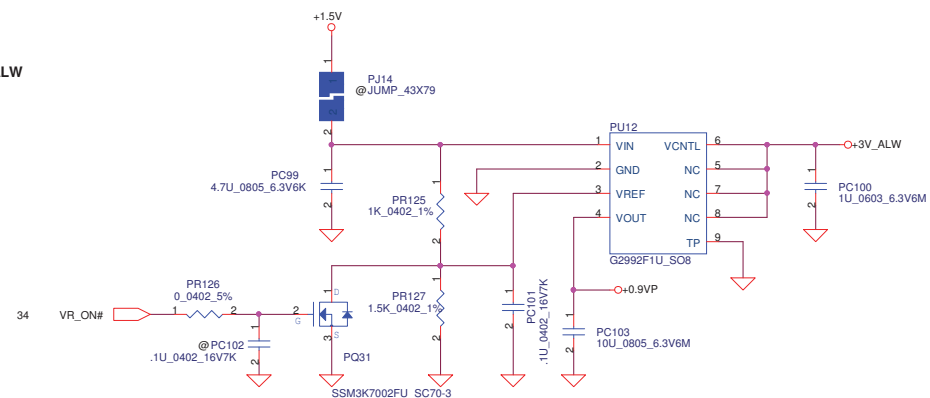
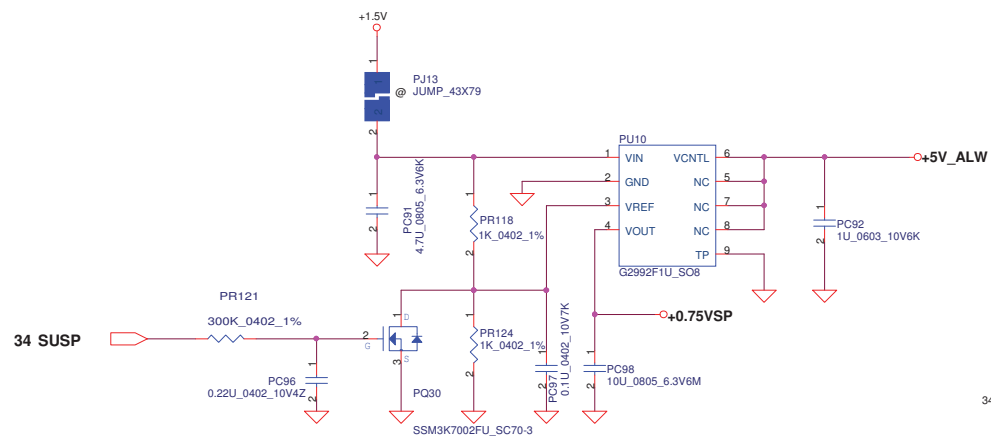
Security Classification	Compal Secret Data			Title	
Issued Date	2009/10/02	Deciphered Date	2010/10/02	+1.1VALWP/+NB COREP	
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I_{peak} = 8A
 I_{max} = 5.6A
 F = 313kHz
 Total Capacitor = 880 uF
 ESR = 5.67m Ohm



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Ipeak = 1.3A

Imax = 0.91A

Total Capacitor = 44 uF

ESR = 2.5m Ohm

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Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
		2009/11/10	POWER		Release
P38	BATTERY CONN / OTP	2009/12/03	POWER	PR31 change to 34.8k	DVT
P38	BATTERY CONN / OTP	2009/12/03	POWER	PR32 change to 15.4k	DVT
P38	BATTERY CONN / OTP	2009/12/03	POWER	PR37 change to 22k	DVT
P38	BATTERY CONN / OTP	2009/12/03	POWER	PR38 change to 10.2k	DVT
P39	CHARGER	2009/12/03	POWER	PC24,25,26 size change to 4.7uf 0805	DVT
P43	0.75VSP/0.9VP/1.8VSP	2009/12/03	POWER	PR121 change to 300k	DVT
P43	0.75VSP/0.9VP/1.8VSP	2009/12/03	POWER	PC96 change to 0.22uf	DVT
P43	0.75VSP/0.9VP/1.8VSP	2009/12/03	POWER	PR125 change to 1k	DVT
P43	0.75VSP/0.9VP/1.8VSP	2009/12/03	POWER	PR127 change to 1.5k	DVT
P44	+CPU_CORE	2009/12/03	POWER	Delete PR142	DVT
P44	+CPU_CORE	2009/12/03	POWER	PR131, PR145 change to 2.2 ohm	DVT
P44	+CPU_CORE	2009/12/03	POWER	PR132 change to 4.7_1206_5%	DVT
P44	+CPU_CORE	2009/12/03	POWER	PC112 change to 680P_0603_50V7K	DVT
P39	CHARGER	2010/01/29	POWER	Add PC47,68,69,127 10U_1206_25V6M	PVT
P41	+1.1VALWP/+NB_COREP	2010/02/03	POWER	Add PC70 4.7U_0805_25V6-K	PVT
P41	+1.1VALWP/+NB_COREP	2010/02/03	POWER	PL9 change to 1.8UH_9.5A_30%	PVT
P44	+CPU_CORE	2009/12/03	POWER	PL13 change to 4.7UH_4A_20%	PVT
P37	CHARGER	2009/02/08	POWER	Move PR18,PR19 to connect PBJ1	PVT2

Item	Reason for change	PG#	Modify List	Date	Phase
1	Update JSATA1, JHDMI1 and JREAD1 footprint		ME request	2009/12	EVT->DVT
2	Update DDR_CS0_DIMMB#, DDR_CS1_DIMMB# net	P06	Net contact error on DIMMB	2009/12	EVT->DVT
3	Update DDR_CKE0_DIMMA, DDR_CKE1_DIMMA net	P06	Net contact error on DIMMA	2009/12	EVT->DVT
4	R41~R44 SMT-->@	P07	Fine tune HDT debug pull high R	2009/12	EVT->DVT
5	Del R46 and add R850-R854	P07	For ESD request	2009/12	EVT->DVT
6	Add RS15 RS16 for NBGFX_CLK,NBGFX_CLK#	P12	For internal clock gen	2009/12	EVT->DVT
7	Fine tune RS880M clock	P12	For internal clock gen	2009/12	EVT->DVT
8	Del external clock gen	P16	For internal clock gen	2009/12	EVT->DVT
9	Fine tune pin define JP4 Pin1 Pin2 Pin8-->GND	P17	Add more GND pin	2009/12	EVT->DVT
10	Add R855 R856 for HDMI_SDATA,HDMI_SCLK pull high R	P19	Solve HDMI can not detect	2009/12	EVT->DVT
11	U6 pin5 +5VL-->+5VS and HDMI Dual NMOSx2(Q6 Q7)->Single NMOS (Q6)	P19	Cost down plan	2009/12	EVT->DVT
12	Add RS1~RS14 near SB820M and TP34 TP35	P20	For internal clock gen	2009/12	EVT->DVT
13	C640 @-->22P on CLK_PCI_EC	P20	EMI request	2009/12	EVT->DVT
14	C705 C705 @-->SMT on Y6	P20		2009/12	EVT->DVT
15	R152 R153 R154 pull +3VALW-->pull GND	P21	Follow AMD check list 1.03	2009/12	EVT->DVT
16	Add device clock request pin on SB820M	P21	For internal clock gen	2009/12	EVT->DVT
17	C632 @-->33P on AZ_BITCLK_HD	P21	EMI request	2009/12	EVT->DVT
18	Add WLAN_PWR_EN# and WWAN_PWR_EN# net on SB820M	P22	Power saving request	2009/12	EVT->DVT
19	U47 +3VL-->+3VALW and Y3 R164 C246 C247 SMT->@	P22	25MHz by default	2009/12	EVT->DVT
20	Reaserved R859 C707 on CLK net	P22	EMI request	2009/12	EVT->DVT
21	Fine tune SB820M strap pin	P24	For internal clock gen	2009/12	EVT->DVT
22	Add C706 0.1u on CLK_PCI_EC	P24	EMI request	2009/12	EVT->DVT
23	Del R193 and Add R858 PH on USB_OC#2	P25	Solve the USB hang up issue	2009/12	EVT->DVT
24	Reserved RM5 RM6 CM17 QM1 RM9 for +3V_WWAN power saving	P26	Power saving request	2009/12	EVT->DVT
25	Reserved RM7 RM8 CM18 QM2 RM10 for +3V_WLAN power saving	P26	Power saving request	2009/12	EVT->DVT
26	Reserved CM19 QM3 RM11 for +1.5V_WLAN power saving	P26	Power saving request	2009/12	EVT->DVT
27	RL21 pin2 +3V_LAN-->GND	P27	LAN vender request	2009/12	EVT->DVT
28	Del RA4 RA5	P28	Fine tune Audio HP out voltage	2009/12	EVT->DVT
29	Reserved RA27 CA26 on AZ_RST_HD#	P28	ESD request	2009/12	EVT->DVT
30	Add Q37 R860 R861 and PD# net	P28	Solve Audio PD# control issue	2009/12	EVT->DVT
31	Fine tune JP5 pin define	P29	Solve the USB hnag up issue	2009/12	EVT->DVT
32	Fine tune SPK_L1,SPK_L2,SPK_R1 and SPK_R2 for SPK	P29	Solve SPK pin issue	2009/12	EVT->DVT
33	Add R857 PH USB_OC#0 net	P29	Solve the USB hnag up issue	2009/12	EVT->DVT
34	Add C708 on +5VS	P29	ESD request	2009/12	EVT->DVT
35	Fine tune card reader pin define	P30	ME use new card reader connector	2009/12	EVT->DVT
36	Add EC_MUTE# on KBC926 (U12) 83pin	P31	Solve Audio PD# control issue	2009/12	EVT->DVT
37	Q8 Q9 R258 R259-->@, R790 R791-->SMT	P33	Cost down plan	2009/12	EVT->DVT
38	C386 @-->0.1u on ON/OFFBTN#	P33	EMI request	2009/12	EVT->DVT
39	C410 0.01u_0402_16V-->0.1u_0603_25V and R267 330k->1M	P34	SMT memo	2009/12	EVT->DVT
40	SYSON#-->SUSP on Q26 Pin2	P34	+0.75VS discharge control pin	2009/12	EVT->DVT
41	RA26 0ohm-->Bead (SM010017710) on INT_MIC_CLK	P28	EMI request	2009/12/18	EVT->DVT
42	C632 @-->33P on AZ_BITCLK_HD	P21	EMI request	2009/12/18	EVT->DVT
43	R788 @-->100ohm and C634 @-->100P on SPI_CLK	P32	RF request	2009/12/18	EVT->DVT
44	R789 @-->100ohm and C635 @-->100P on AZ_BITCLK_HD	P28	RF request	2009/12/18	EVT->DVT
45	Add CA63 on INT_MIC_CLK_R	P28	RF request	2009/12/18	EVT->DVT
46	RA1 0ohm-->Bead on Audio power	P28	RF request	2009/12/18	EVT->DVT
47	Add CM20 1000P on +3V_WWAN	P26	RF request	2009/12/18	EVT->DVT
49	Add C709 on 27M_SEL	P16	RF request (EXT only)	2009/12/19	EVT->DVT
49	Fine tune R133 R value 11.8K-->8.2K	P21	Fine tune USB signal	2009/12/22	EVT->DVT
50	<BOM>RA22 RA25 4.7K-->2.2K and CA16 10u-->@	P28	Audio vender request	2009/12/22	EVT->DVT
51	Add BT_PWR# net contact to JWLAN1 pin5	P26	Follow common design	2009/12/23	EVT->DVT
52	Del R161 and SLP_CHG on SB	P22	Follow common design	2009/12/23	EVT->DVT
53	Add SLP_CHG on pin115 and add R862	P31	Follow common design	2009/12/23	EVT->DVT
54	Add UA2 CA67 CA68 CA69	P28	Audio power reserved	2009/12/23	EVT->DVT
55	Add F2 for card reader proetct	P30	H/W request	2009/12/24	EVT->DVT
56	Reserved RA28 CA70	P28	Reserved for fin tune aduio power control	2009/12/24	EVT->DVT
57	Add R863 PH on CIR_EN#	P21	Follow common design	2009/12/24	EVT->DVT
58	Add R864 on LID_SW#	P33	Reserved for ESD protect	2009/12/24	EVT->DVT
59	Modify TP26 TP27-->EVENT#_A and EVENT#_B	P08 P10	Solve layout test point issue	2009/12/25	EVT->DVT
60	C497 SMT-->@	P08	Fine tune CPU_CORE cap	2009/12/25	EVT->DVT

Item	Reason for change	PG#	Modify List	Date	Phase
1	Add D17 and Q38 for BT power control	P26	Follow common design	2010/1/20	DVT->PVT
2	Change net name SLP_CHG-->SLP_CHG#	P25 P31	Follow net rule	2010/1/20	DVT->PVT
3	Need to fine tune R783 and R784	P18	VB function	2010/1/20	DVT->PVT
4	<BOM> SB use 2MB SPI ROM SA00002TO00	P22	Non share ROM	2010/1/20	DVT->PVT
5	<BOM> Update LAN P/N for LAN VB P/N	P27	Vender update P/N	2010/1/20	DVT->PVT
6	<BOM> EC SPI use 256KB SPI ROM SA00003GK00	P32	Non share ROM	2010/1/20	DVT->PVT
7	BT part SMT-->@	P29	IUR no BT device	2010/1/20	DVT->PVT
8	Update JREAD1 footprint (Same as EVT)t	P30	ME request	2010/1/20	DVT->PVT
9	Update JSATA1 footprint TAIWI_EU114-117CRL-TW_11P-T	P25	ME request	2010/1/20	DVT->PVT
10	Update JHDD1 pin4 +5VS-->GND	P25	HW request	2010/1/20	DVT->PVT
11	Del DC to DC +NB_CORE part	P34	HW request	2010/1/20	DVT->PVT
12	Change USB port10 to USB port5 on WWAN	P21	Follow common design	2010/1/20	DVT->PVT
13	Add R865 R866 for SLP_CHGX_M3/M4 on SB	P21	Follow common design	2010/1/20	DVT->PVT
14	Add R867 R868 for SLP_CHGM3/M4 on EC	P31	Follow common design	2010/1/21	DVT->PVT
15	UA2 pin5 +PVDD1--->+AVDD	P28	Reserved for Audio analog power	2010/1/21	DVT->PVT
16	<BOM> U48 SA000008G00-->SA00003DR00 (Same as intel)	P29	HW request	2010/1/21	DVT->PVT
17	Del R164 Y3 C246 C247 and add TP36 TP37	P22	HW request	2010/1/22	DVT->PVT
18	JLVDS1 pin24 +LCD_INV-->NG	P18	Follow common design	2010/1/22	DVT->PVT
19	U9 pin1 +5VALW-->+5V_ALW for USB charge	P25	Follow common design	2010/1/22	DVT->PVT
20	Add C900~C908,R900~R906 Q40 Q41 U49 U50 for power save	P34	Follow common design	2010/1/22	DVT->PVT
21	Update JTP1 footprint--> E-T_6916-Q06N-00R_6P	P33	ME request	2010/1/25	DVT->PVT
22	Update USB20_P10-->USB20_P5_USB20_N10-->USB20_N5	P21 P26	Follow common design	2010/1/25	DVT->PVT
23	Update JHDMI1 footprint-->SUYIN_100042GR019M23BZR_19P-T	P19	ME request	2010/1/25	DVT->PVT
24	R900 pin 1 and R904 pin1 +B-->+VSB	P34	HW request	2010/1/27	DVT->PVT
25	Add J2 J3 for +3V_ALW and +5V_ALW	P34	HW request	2010/1/27	DVT->PVT
26	R808 pin 1,R809 pin2 +3VALW-->+3V_ALW and +5VALW-->+5V_ALW	P33	HW request	2010/1/27	DVT->PVT
27	Add R907 for USB_EN# PH	P29	HW request	2010/1/27	DVT->PVT
28	Del R808 R809 R811 R810 R258 Q8 R259 Q9	P33	HW request	2010/1/27	DVT->PVT
29	R238 pin1 +3VALW-->+3V_ALW	P31	HW request	2010/1/29	DVT->PVT
30	JTP1 pin1 +3VALW-->+3V_ALW	P33	Follow common design	2010/1/29	DVT->PVT
31	Del R246	P32	HW request	2010/1/29	DVT->PVT
32	Add LPC_FRAME#, LPC_AD, LPC_AD1,LPC_AD2,LPC_AD3 JWAN1	P26	HW request	2010/1/29	DVT->PVT
33	Update JPB1 footprint P-TWO_161011-04021_4P-T	P33	ME request	2010/1/29	DVT->PVT
34	Add JHDD2 ACES_87036-1001-CP_10P	P25	HW request	2010/1/29	DVT->PVT
35	Fine tune JP4 pin define for EMI request	P17	EMI request	2010/1/29	DVT->PVT
36	<BOM> Update UA1 P/N for Audio VB version	P28	Vender update P/N	2010/1/29	DVT->PVT
37	Update JP5 pin define and 20pin-->22pin	P29	HW request	2010/1/30	DVT->PVT
38	<BOM> R133 8.2K-->11.8K same as EVT	P21	HW request	2010/1/31	DVT->PVT
39	Add C909 C910	P17	EMI request	2010/1/31	DVT->PVT
40	Add D18 and R908 on RTC circuit	P20	Follow common design	2010/1/31	DVT->PVT
41	JHDD1 10pin-->12pin	P29	Add more power and GND pin on HDD conn	2010/1/31	DVT->PVT
42	Add R909 R910 for ADAPTOR_SEL	P31	Follow common design	2010/1/31	DVT->PVT
43	Add L41 L42 L43 C911 C912 C913 for EMI request	P12	EMI request	2010/2/2	DVT->PVT
44	C240 C244 22P to 18P	P20	Solve RTC fial issue	2010/2/2	DVT->PVT
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